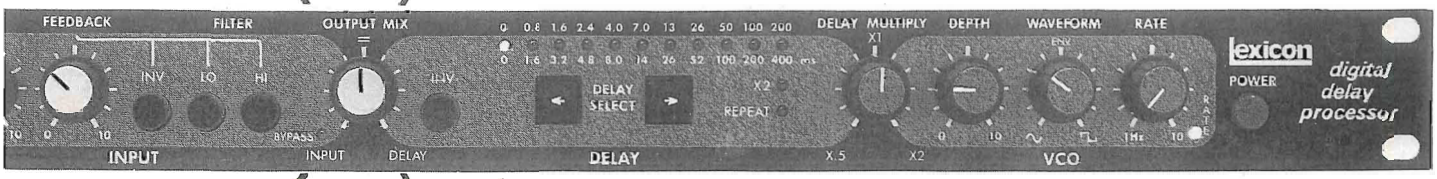


pcm 41

digital delay processor

SERVICE MANUAL

Lexicon

Lexicon, Inc., 60 Turner Street
Waltham. Mass. 02154/617-891-6790

Bill Orner

5.1.16 Output Mixer
5.1.17 Bypass Switch
5.1.18 Output Stage

5.2 VCO and LFO
5.2.1 Clock Oscillator
5.2.2 Depth and Waveform Controls
5.2.3 Delay Multiply Control
5.2.4 Envelope Follower
5.2.5 Waveform Generator

5.3 Digital
5.3.1 Address Offset Logic Basics
5.3.2 Timing Generation
5.3.3 Address Counter
5.3.4 Delay Select Logic
5.3.5 Adder Logic
5.3.6 Address Multiplexer
5.3.7 Memory
5.3.8 Bus Logic
5.3.9 Conversion Logic

5.4 Power Supply

6.0 Reference Section

6.1 Interior Layouts

6.2 Schematics
6.2.1 Analog
6.2.2 Converter
6.2.3 Digital
6.2.4 VCO/Power Supply

6.3 Parts Lists
6.3.1 Chassis
6.3.2 Motherboard
6.3.3 Headroom Indicator P.C. Board
6.3.4 Delay Select (Display) P.C. Board

6.4 I.C. Layouts

6.5 Signature Analysis Tables

7.0 Repair Return

7.1 Parts Replacement

7.2 Warranty

TABLE OF CONTENTS

1.0 Introduction
1.1 Equipment Required
1.2 Description
1.3 Specifications

2.0 Inspection
2.1 Power-up
2.2 Performance Tests
  2.2.1 Input Gain, Headroom Indicator
  2.2.2 Output Level, Distortion
  2.2.3 Signal-to-Noise
  2.2.4 Frequency Response
  2.2.5 Feedback, Mix Out, Invert Switches
  2.2.6 Delay Time
  2.2.7 VCO Section
  2.2.8 External Jacks

3.0 Calibration
  3.0.1 Power Supply
  3.0.2 VCO Calibration
  3.0.3 Converter Calibration
  3.0.4 Filter Calibration
  3.0.5 Mix Control Calibration
3.1 Voltage Changeover
3.2 RFI Option

4.0 Troubleshooting
4.1 Check Power Supply
4.2 Unit Functions Only at "0" Delay
4.3 Noise Increases with Delay
4.4 Distortion at "0" Delay: Converter
4.5 Filter Problems
4.6 Signature Analysis Testing

5.0 Theory of Operation
5.1 Theory of Operation - Analog
  5.1.1 Input Stage
  5.1.2 Input Filter
  5.1.3 Pre-emphasis Network, Input Mixer
  5.1.4 Headroom Indicator
  5.1.5 Sample/Hold
  5.1.6 Log Circuit
  5.1.7 A to D Converter
  5.1.8 D to A Converter
  5.1.9 Anti-Log Circuit
  5.1.10 Output Deglitcher
  5.1.11 Aperture Correction Filter
  5.1.12 Inverter
  5.1.13 Feedback
  5.1.14 De-emphasis Network
  5.1.15 Output Filter

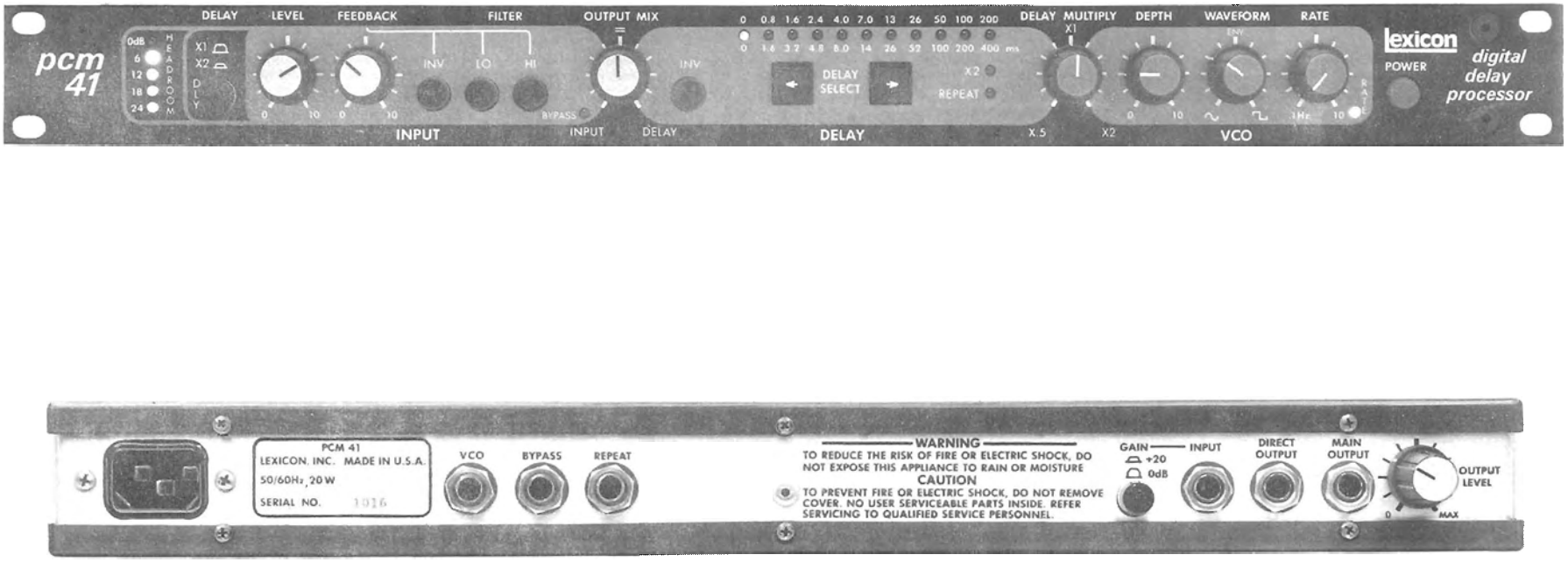


FIG. 1.0 FRONT & REAR PHOTOS

1.0 INTRODUCTON

This manual provides service and maintenance information for the Lexicon PCM-41 Digital Delay Processor. It is intended for use by qualified service personnel. Efficient service requires a basic understanding of both analog and digital circuits, as well as most of the equipment listed below. Routine calibration or verification of performance may be accomplished with only a few pieces of test equipment. In the event that repair or calibration cannot be performed in the field, the unit may be returned to the factory for service (see section 7.0).

1.1 EQUIPMENT REQUIRED

The following list of test equipment will be helpful or necessary for calibration or repair of the PCM-41:

a) D.C. - 15 MHz dual trace scope with D.C. triggering such as Tektronix T922, Hewlett-Packard 1220A, or Philips 3226.
b) Low distortion (< .02%) sine-wave oscillator such as Hewlett-Packard 339A or Tektronix SG505.
c) Harmonic distortion analyzer with .01% resolution such as Hewlett-Packard 339A or Tektronix AA501.
d) A.C. voltmeter with 300 microvolt full-scale sensitivity.
e) Digital voltmeter.
f) Frequency counter.
g) Pulse generator for delay time measurements.
h) Signature Analyzer, Hewlett-Packard 5004A or equivalent.
i) A variac with voltmeter and ammeter.

In addition, a full complement of analog and digital IC's is useful for substitution when a fault has been isolated to a particular circuit section.

1.2 DESCRIPTION

The PCM-41 is a single channel digital delay line useful for audio signal processing or modification. It was designed for performing musicians or recording studios for the modification of musical instrument sounds. The front panel contains three basic groups of controls: audio level and mixing, delay selection, and time base sections.

In the audio section, controls are provided for setting input level, delayed feedback level, and the output mix of direct and delayed signals. Also, switches are provided for feedback phase inversion, high and low pass feedback filters, and delay output phase inversion. Delay selection is accomplished by means of up and down pushbuttons allowing one of eleven possible delay settings, a 2X delay switch which doubles delay at the expense of audio bandwidth reduction, and a delay multiply control which gives a 4:1 change of the basic pushbutton selected delay. Dynamic modification of the delay time (VCO section) is possible using the low frequency oscillator (LFO) which

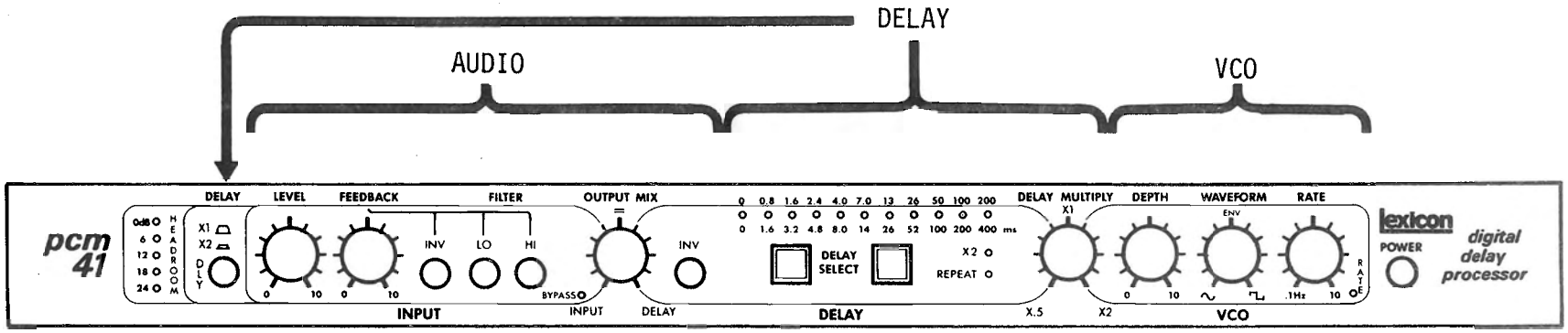


FIG. 1.2

FRONT PANEL CONTROL GROUPING

produces sine or square waveforms at a rate adjustable from 0.1 Hz to 10 Hz. The depth of delay modulation is continuously adjustable from 0 to 100% (4:1).

Also available is an envelope waveform derived from the rectified input signal at the headroom indicator. This may be used to modulate the delay and may be blended with the sine or square wave from the LFO through the waveform control. At the rear of the unit are input and output jacks for the audio signal and an output level control for matching levels to following equipment. An input 20 dB gain switch allows interface with low output signal sources such as musical instrument pickups. Three more jacks at the rear allow footswitches to control delay bypass and memory repeat functions and allow external signal sources to modulate delay.

1.3 SPECIFICATIONS

Total Distortion and Noise

0.04% typical, 0.07% maximum @ 1 kHz, DELAY & DELAY MULTIPLY = X1
0.1% typical over bandpass of 20 Hz to 15 kHz.

Frequency Response

20 Hz to 15 kHz, +0, -1 dB in X1 mode.
10 Hz to 16 kHz, +0, -3 dB in X1 mode.
20 Hz to 6.0 kHz, +0, -3 dB in X2 mode.

Dynamic Range

Better than 90 dB, 20 Hz-20 kHz noise bandwidth.

Delay Capacity

DELAY MULTIPLY = X1:	200 milliseconds at full bandwidth;
	400 milliseconds at 6 kHz bandwidth.
DELAY MULTIPLY = X2:	400 milliseconds at full bandwidth;
	800 milliseconds at 6 kHz bandwidth.

Delay Selection

11 pushbutton selected taps; each tap is continuously variable over a 4:1 range via the Delay Multiply control. Taps are at: 0, 0.8, 1.6, 2.4, 4, 7, 12, 26, 50, 100 and 200 ms in DLY X1 mode (double these times in DLY X2 mode).

VCO Modulation

Depth is adjustable from 0 (none) to a 4:1 sweep of delay time. Rate is adjustable from 0.1 Hz to 10 Hz. An LED flashes to indicate VCO modulation rate.

VCO Shape

Continuous adjustment is available between Sine wave and Envelope, or Square wave and Envelope functions.

Input Type

Balanced differential input, via standard 1/4" Tip-Ring-Sleeve phone jack, offers 40 dB common mode rejection. Will also accept unbalanced input.

Input Impedance

Balanced or unbalanced input; 40K ohms impedance.

Input Level

With adjustable INPUT LEVEL control and 20 dB GAIN switch on rear panel, maximum input levels of from -23 dBV to +19 dBV (0.07 V to 9 V rms) can be accommodated (the 0 dBV reference is 1.0 volts rms).

Output Type

Both Main and Direct outputs are unbalanced, and have standard 1/4" Tip-Sleeve phone jacks.

Output Impedance

Main Out: 100 ohms actual source impedance.
Direct Out: 600 ohms actual source impedance.
Both outputs are intended for driving high impedance loads, but are operable with loads as low as 600 ohms.

Output Level

Main Out: +19 dBV (9 V rms) maximum. Will drive loads of 2K ohms or greater at full level. An Output Level control varies the level.
Direct Out: Level depends only on Input Level and 20 dB Gain switch; when Headroom indicates 0 dB, output level is +11 dBV (3.5 V rms).

Remote Jacks

Rear panel 1/4" phone jacks accomodate external switches and controls as follows:
Bypass: When the Tip and Sleeve of the mono phone jack are shorted together, the PCM-41 is placed in bypass mode.
Repeat: When the Tip and Sleeve of the mono phone jack are momentarily shorted, the PCM-41 captures a brief segment of the input and holds it in repeat mode. A subsequent momentary contact of Tip and Sleeve releases the segment, returning the unit to normal operation.
VCO: This stereo phone jack may be connected to a potentiometer or a voltage source; whenever a plug is inserted in the jack, the Delay Multiply control is replaced by the external device. A pot resistance from 10K to 500K ohms (50K ohms ideally), should be used, Tip wired to the wiper, Ring and Sleeve to the pot inputs. A positive voltage source of 0 to 10 V can feed the Tip, with Ring and Sleeve connected to the common.

Headroom Indicator

5 LEDs display input level in 6 dB steps. The upper limit of "0 dB" is the point at which the analog to digital converter clips.

Remote Indicators

Bypass and Repeat LEDs on the front panel are illuminated when the respective functions have been activated via the remote input jacks.

Delay Range

A latching pushbutton selects X1 or X2 range (200 ms or 400 ms maximum indicated delay); an LED is illuminated in X2 mode. The Delay Select pushbuttons increment the nominal delay time up and down, as shown by the 11 Delay Time LEDs.

Mixing Controls

Level controls are provided for the Input and Feedback circuits. Feedback also includes its own Invert (polarity) switch and Lo cut (80 Hz) and Hi cut (4 kHz) filters. The Main Output is provided with an Output Mix control to blend direct and delayed sound (center detent for equal blend), a delay Invert switch, and an Output Level control.

AC Requirements

115 or 230 volts (selectable), 50 or 60 Hz, 20 watts maximum. Standard IEC power connector on rear of unit; 3-prong cord provided.

Protection

Mains are fused (standard U.S. 3AG fuses).

Export Models

Mains and secondaries are fused (European 20 mm fuses). An RFI power line filter is also installed. NOTE: A 100 volt export model is available on special order.

Dimensions

Standard 19" relay rack mount (483 mm).
1-3/4" high (44 mm) by 11" deep (280 mm).

Weight

Net, 5.5 lbs. (2.5 kg); shipping, 8 lbs. (3.6 kg).

2.0 INSPECTION

Before applying power to the PCM-41, check the setting of the mains voltage selector switch. This switch is located inside the unit near the power switch. Be sure the correct fuse(s) have been installed. Also be sure to check for 100 volt option which will be identifiable by the Lexicon part number on the power transformer (see parts list in section 6.0). The mains voltage for which the unit was set at the factory appears on a small sticker at the outside rear of the chassis to the right of the mains connector.

2.1 POWER UP

When the unit is first turned on, the "0" DELAY light should be on and the REPEAT light off. The RATE light should flash on and off at a rate determined by the RATE control. If no audio signal is present, the Headroom Indicator lights should be off regardless of the setting of Input Level or +20 dB GAIN switch. If the Delay X2 button is depressed, the X2 light will come on. If no footswitches are connected, the BYPASS light will remain off.

2.2 PERFORMANCE TESTS

If the unit powers up correctly, set the three controls in the audio section full counterclockwise, all front panel pushbuttons out, DELAY MULTIPLY control to X1 and DEPTH to 0 (CCW). Set GAIN switch on rear panel to +20 dB (switch in).

2.2.1 Input Gain, Headroom Indicator

Apply a 1 kHz, low distortion sine wave to the INPUT at a level of -20 dBm (.0774 volts). The "24 dB" headroom light should be on. Advance the INPUT LEVEL control to full clockwise. All headroom lights should light in sequence.
Set rear panel GAIN switch to 0 dB (switch out), and increase sine wave input level until "0 dB" light just comes on. Input level should be -1 dBm +/-1 dB (0.7 volts).

2.2.2 Output Level, Distortion

Connect an A.C. voltmeter and harmonic distortion analyzer to the MAIN OUTPUT. Adjust OUTPUT LEVEL control on rear panel for a level of +10 dBm (2.44 volts). Distortion in direct mode should be less than .03%. Rotate OUPTUT MIX control to full clockwise position. Distortion should be less than .07%. If clipping occurs, reduce input slightly until distortion drops. Then readjust OUTPUT LEVEL control.Using the DELAY SELECT buttons, step through the ten delay settings while monitoring distortion. When the maximum delay is reached, depress the DELAY switch (to

the left of the INPUT LEVEL control) and step back to "0" DELAY. The distortion should never exceed .07% for these settings. With the DELAY switch in, rotate te DELAY MULTIPLY control through its range (X0.5 to X2). Distortion should not exceed 0.1% with the highest reading appearing at DELAY MULTIPLY X2. With DELAY switch at X1, distortion may reach 1% at DELAY MULTIPLY control setting of X2. This is primarily clock feedthrough and should decrease to less than 0.1% for DELAY MULTIPLY settings less than X1.5.

2.2.3 Signal To Noise

Return DELAY MULTIPLY control to X1. Remove sine wave and short circuit the INPUT. Output noise with OUTPUT MIX control in DELAY position (CW) should be -80 dBm or less and in INPUT position -85 dBm as measured with a 20 Hz - 20 kHz DIN filter. A voltmeter with wideband response will give readings about 6 dB higher. Be sure both covers on the PCM-41 are secure.

2.2.4 Frequency Response

Set OUTPUT MIX control to DELAY position. Using an input level which just lights the "12 dB" headroom light at 1 kHz, measure the frequency response of the unit. From 20 Hz to 15 kHz, this should be within 1 dB, dropping to -3 dB at about 16 kHz. The direct or BYPASS path should be flat within 1 dB from 20 Hz - 20 kHz.

2.2.5 Feedback, Mix Out, Invert Switches

Apply a 1 kHz signal of -10 dBm to the input. While monitoring the MAIN OUTPUT with an A.C. voltmeter, turn the FEEDBACK control full clockwise. The output should increase about 10 dB. Switching in the LO FILTER will cause the output to increase about another 2 dB. Switching in the HI FILTER will cause about a 4 dB decrease in output. Switching in the FEEDBACK INV will cause about a 15 dB decrease in output. Return the FEEDBACK control to full counterclockwise position.
Apply a 100 Hz signal to the INPUT and adjust level until "0 dB" headroom light comes on. Observe MAIN OUTPUT level on A.C. voltmeter. Rotate OUTPUT MIX control to "=" (mid position). Output level should remain unchanged. Depress DELAY INV switch (to right of mix control). Output should decrease about 30 dB. Connect A.C. voltmeter to DIRECT OUTPUT. Reading should be +13 dBm +/-1 dB with "0 dB" headroom light just lit.

2.2.6 Delay Time

Connect a pulse or tone burst generator to the INPUT and a triggered sweep oscilloscope to the MAIN OUTPUT of PCM-41. Connect the oscilloscope EXTERNAL TRIGGER to the pulse generator output or TRIGGER output. Set the OUTPUT MIX control of the

PCM-41 to "=" (mid position). Adjust the 'scope to trigger on the leading edge of the pulse. This will allow the input pulse followed by the delayed pulse to be displayed on the oscilloscope. Using a 100 microsecond to 1 millisecond pulse or several cycles of 10 kHz tone burst with a repetition rate of once per second, step through the ten delay settings and verify that the delay times are within +/-10% of the indicated values. Note that "0" delay is actually about 100 microseconds, the residual delay of the low/pass filters and converter. Verify the operation of the DELAY MULTIPLY control and check delays at its two extremes of rotation. Verify that the DELAY switch doubles delay time.

2.2.7 VCO Section

Using the set-up of the previous section, check the operation of the three remaining VCO controls. Set the DELAY MULTIPLY control to "X1" and select a delay and 'scope sweep to place the delayed pulse at the center of the 'scope screen. Set the RATE control full counterclockwise, the WAVEFORM control clockwise to "⌐⌐" and rotate the DEPTH control clockwise to "10". The delayed pulse should jump back and forth from about 25% to 100% of the sweep time spending about 5 +/-1 seconds at each position. Rotate the WAVEFORM control counterclockwise to the ENV (mid position). The delayed pulse should be displaced from the center of the screen toward the original (input) pulse. The amount will vary depending on the selected delay time. Continue rotating the WAVEFORM control counterclockwise to "⌐⌐". The delayed pulse should now move smoothly back and forth from 25% to 100% of the sweep time. Rotating the RATE control clockwise to 10 Hz will cause the delayed pulse to move rapidly back and forth. Note that as the low frequency oscillator rate exceeds the repetition rate of the pulse generator, the delayed pulse will appear to move randomly on the 'scope screen.

The above tests may be performed using a continuous sinewave input source. The effect of the low frequency modulation will be to frequency modulate the sinewave source from about one octave up to one octave down from the original frequency.

2.2.8 External Jacks

External or remote operation requires a single pole momentary closure switch for REPEAT function, a single pole normally open switch for BYPASS function and a 50k potentiometer for EXT. VCO control. The first two functions are not operable from the PCM-41 front panel. The EXT. VCO control, normally a foot pedal (available as an option - Lexicon part no. 750-02432), allows remote control of DELAY MULTIPLY. The pot is wired to a stereo phone plug, the ends of the element to ring and sleeve, the wiper to the tip. Refer to section 2.2.6 for checking operation of DELAY MULTIPLY control. To check REPEAT function connect a signal source to the PCM-41 INPUT and adjust source for convenient input

level. Operate momentary closure switch once and observe that REPEAT light on front panel lights and stays lit. Disconnect input source and using 'scope or listening to delayed output, verify that signal is still present (DELAY SELECT must be other that "0"). A small click may be heard, repeating at the basic memory length of the machine. To change this length, the DELAY switch must be depressed and/or the DELAY MULTIPLY control changed. Changing these controls will now alter the pitch of the repeated segment. A second closure of the REPEAT switch will extinguish the REPEAT light and erase the stored segment.

To check the BYPASS function, connect a signal source to the PCM-41 INPUT and adjust source for convenient input level. Set OUTPUT MIX control to DELAY position and DELAY SELECT to some delay. Use VCO section to produce modulation of input signal. Close BYPASS switch and observe that BYPASS light (to left of OUTPUT MIX control) illuminates. Using scope or listening to output of machine, verify that original input signal only is present at output. Opening BYPASS switch should extinguish BYPASS light and restore modulated input signal.

3.0 CALIBRATION

Calibration is initially done at the factory and should be good for the life of the machine. Should component replacement become necessary, the affected circuit may need recalibration. Replacement of a power supply regulator may necessitate recalibration of the VCO or converter section. For this reason, the calibration procedure is hierarchical and should be performed in the order listed.

3.0.1 POWER SUPPLY

Connect the PCM-41 to a suitable source of power. A variac with voltmeter and ammeter is useful for determining input voltage for power supply regulator dropout and verifying input power to be within specification. Should the unit under test be wired for a voltage other than that available, the voltage changeover switch inside and fusing may be changed to accomodate the local mains. Likewise, if a variac is available, 100 volt units may be operated from 115 volt mains and vice versa. It is also possible to operate 100 volt units on 240 volt mains by means of the voltage changeover switch (which would give a unit a nominal 200 volt requirement). Be sure to return switch and fusing to correct values after calibration.

Set variac to nominal operating voltage and power up PCM-41. Current drain should be less than 0.15 amp at 115 VAC 60 Hz. This current will vary inversely proportional to nominal operating voltage. In all cases, power drain should be less than 20 watts.

There are six regulated power supply voltages in the PCM-41. Five of these are accessible at test points near the center rear of the printed circuit board. The sixth is in the VCO section near the right front. Refer to figure 3.0 for locations of all test and calibration points. The following table gives minimum and maximum acceptable values for the six voltages. Since there are no adjustments for these regulators, an out of tolerance voltage may be caused by a defective regulator or excessive current drain on that supply.

	Min. Voltage	Max. Voltage
+5 volt Logic Supply	+4.75	+5.25
+12 volt Memory Supply	+11.40	+12.60
-5 volt Memory Supply	-4.50	-5.50
+15 volt Analog Supply	+14.25	+15.75
-15 volt Analog Supply	-14.25	-15.75
+5 volt Analog (VCO) Supply	+4.50	+5.50

CAUTION: Failure (short circuit) of -5 volt supply may cause permanent damage to 16k memory IC's.

Reduce variac voltage by 10%. All supplies should remain stable to within 1% of nominal line values.

3.0.2 VCO CALIBRATION

Connect oscilloscope and frequency counter to collector of Q6 (refer to VCO schematic in section 6.2). Some counters load their sources heavily. The scope is to check quality and symmetry of the signal, MCO. This waveform should be square, symmetrical to within +/-15%, and have an amplitude of about 4 volts with the low level being at +0.5 volts +/-0.5 volt. Set the front panel DEPTH control to "0" and DELAY MULTIPLY to "X2". Adjust R141 for a counter frequency reading of 343 kHz +/-10 kHz.
Set DELAY MULTIPLY control to "X0.5" and adjust R137 for frequency of 1.31 MHz +/-20 kHz.
Set DELAY MULTIPLY control to "X1.0" and adjust R136 for frequency of 655 kHz +/-10 kHz.
Set RATE control to "0.1 Hz", DEPTH control to "10", and WAVEFORM control to " ⌐⌐ ". Counter will deviate back and forth between two frequencies at a rate of 5 seconds each. Observe that the two frequencies correspond to the "X2" and "X.5" settings within +/-10%. Failure of this test indicates a problem in the waveform generator. Refer to Theory of Operation section 5.2.

3.0.3 CONVERTER CALIBRATION

Connect low distortion, 1 kHz sine wave signal source to INPUT. Set level to 0 dBm. Connect harmonic distortion analyzer and oscilloscope to MAIN OUTPUT. Set OUTPUT MIX control to DELAY, DELAY MULTIPLY to "X1", DEPTH to "0", DELAY SELECT to "0", FEEDBACK LEVEL to "0", and adjust INPUT LEVEL until "0 dB" headroom light just extinguishes. Adjust OUTPUT LEVEL on rear panel for about +10 dBm output.
Adjust R82 for minimum distortion.
Reduce generator level 20 dB (or rotate INPUT LEVEL control to "0") and adjust R81 for minimum distortion. Return generator to previous level and readjust R82 for lowest distortion. This should be less than .05% and typically .03%. Raise generator level another 1 dB or so until clipping occurs. This will be "hard" clipping and should be symmetrical (both peaks). Drop generator level 20 dB. Distortion should be less than 0.3%.
Check distortion at various delay settings with DELAY switch in "X2", and with DELAY MULTIPLY in "0.5". If unit fails to meet specification, refer to troubleshooting, section 4.2.

3.0.4 FILTER CALIBRATON

There are two identical 5-pole elliptical filters in the PCM-41, one at the input to prevent aliasing and one at the output to remove clock and other spurious signals. The filter characteristics are: cutoff frequency, 17.3 kHz; passband ripple, 0.5 dB; stopband attenuation, 65 dB. A description and frequency response plot of the filter is shown in section 5.1.

To adjust the input filter, apply a 100 Hz signal from a sine wave generator with at least +/-.1 dB flatness of output across the audio band to the INPUT of the PCM-41. Adjust generator or INPUT LEVEL

control to extinguish the "12 dB" headroom light. Connect an A.C. voltmeter to IC U11, pin 7. Readjust input level for a convenient reference reading on voltmeter. This becomes the "0 dB" reference for the filter response. (Be sure the DELAY switch is in X1 position). Change generator frequency to 10 kHz and adjust R9 for "0 dB" +/-.25 dB reference level on voltmeter. Next set generator to 14 kHz and adjust R8 for "0 dB" +/-.25 dB reference level. Check to see that response is no more than "0.5 dB" down at 6 kHz and 15 kHz. If it is, refer to troubleshooting, section 4.5.

To adjust output filter, leave generator connected to INPUT and set to 100 Hz at previous output level. Connect A.C. voltmeter to MAIN OUTPUT of PCM-41. Be sure FEEDBACK control is at "0", OUTPUT MIX is at DELAY, DELAY MULTIPLY control is at "X1", DEPTH at "0", and DELAY SELECT is "0". Set convenient voltmeter reference with OUTPUT LEVEL control on rear panel. Change generator frequency to 10 kHz and adjust R7 for flatest response. Next, set generator to 14 kHz and adjust R6 for flatest response. Check to see that response is not more than "1.0 dB" down at 6 kHz and 15 kHz. If it is, refer to troubleshooting, section 4.5.

Depress DELAY switch and check machine for response, +/-1.0 dB to 5 kHz. Set generator to 8 kHz. Output should be "-40 dB" or greater. Set generator to 30 kHz and DELAY switch to "X1". Output should be "-40 dB" or greater.

3.0.5 MIX CONTROL CALIBRATION

Keeping setup for filter calibration, set generator to 100 Hz at -2 dBm. Adjust INPUT LEVEL control to just extinguish "0 dB" headroom indicator and OUTPUT LEVEL control to give +10 dBm output. Rotate OUTPUT MIX control to "=". Output level should not change (be sure you have "0" DELAY). Depress DELAY INV switch and adjust R99 for minimum output. It should be possible to achieve at least 30 dB cancellation (-20 dBm output).

3.1 VOLTAGE CHANGEOVER

Voltage conversion from 115 VAC to 230 VAC operation or vice versa, may be performed simply by selecting the appropriate voltage with the voltage changeover switch located inside the PCM-41 near the POWER switch. The mains fuse, F1, must also be changed to the appropriate rating and type. If the unit was originally built for domestic 115V service, this fuse will be a 3AG type; whereas for export, a 5 X 20 mm European style fuse will have been used. Changing the fuse style is not recommended, since the fuse clips will not suitably retain the fuse.

Voltage conversion from or to 100 VAC operation will require a power transformer change. This part is only available from the factory and is listed in the parts list, section 6.3.2. It is not recommended that the machine be run at other than the rated line voltage +/-10%.

Export machines are fused at the transformer secondaries also. These fuses will be 5 X 20 mm types of the same rating regardless of mains voltage. The correct values of all fuses are printed on the main circuit board near the POWER switch.

3.2 RFI OPTION

Export machines are equipped with an RFI filter integral to the mains connector. This option is also available on domestic units on special order. In this case, the secondary fuses will be included. The filter is available from the factory and is listed in the parts list, section 6.3.2.

All phone jack inputs and outputs are bypassed at the jacks as standard to minimize R.F. leakage.

4.2 UNIT FUNCTIONS ONLY AT "0" DELAY

This indicates that the trouble lies in the digital or memory sections of the machine. However, the VCO clock must be functioning, since the converter will not pass audio without basic timing signals. In "0" DELAY mode, the converted 12 bit sample is held by the SAR (successive approximation register, U45) and sent by way of tri-state buffers (U34, U40) to the DAC (U19) for reconversion, indicating that these components are probably OK. The problem may lie in the memory data bus (U33, 35, 39, 41), memory timing (U31), address multiplexers (U37, 43) or adders (U36, 42), or the memory itself. If the signal is totally absent in delay, a basic timing signal is at fault and should be checked with a scope. If it is merely noisy, then one or more memory ICs may be suspect and the memory chips may be swapped around to see if the noise level changes. (A bad chip will give the most noise in U30 position, the least noise in U25 position). Check the main counter chain (U38, 44) with a scope or frequency counter for 2 to 1 frequency division as you proceed down the chain from WC0 to MA13. Be sure to refer to Theory of Operation: Digital, section 5.3 for the machine timing diagram. Trigger the scope from a lower frequency clock than the signals you are verifying; for example, trigger on the signal WC3 to examine all of the timing associated with a sample period.

4.3 NOISE INCREASE WITH DELAY

If noise or distortion increase with increasing delay, the fault is probably with the VCO (voltage controlled oscillator), IC (U59) or associated circuitry. The VCO produces the signal MC0, which is the master clock for the PCM-41. A "clean" clock waveform with very low jitter or time uncertainty is essential to the realization of low noise in the converter. If the clock noise is very low frequency, such as might be produced by a defective IC, the noise will worsen as the delay period is increased. Be sure to replace U59 with a factory approved part. Some manufacturers' parts will not operate satisfactorily in the PCM-41.

4.4 DISTORTION AT "0" DELAY: CONVERTER

Verify that the fault is in the converter section. Remove IC U16 and connect a jumper from U11 pin 1 to U16 pin 1. This will allow the signal to bypass the entire converter section.

If it is determined that the fault is indeed in the converter section, the next things to check are the pertinent timing signals. These are: ISAM/, OSAM/, MC/, SC/, and SARE/. Check to see that comparitor (U20) DATA is reaching the SAR (U45). Check DAC0 through DAC11 lines to U19.

To determine whether the input sample/hold and output deglitcher circuits are at fault, the log, anti-log, and A/D-D/A converter may be bypassed by removing IC U15 and connecting a jumper from U22 pin 6 to U15 pin 6. The signal should pass through with less than .05% distortion. If not, the ICs U16, U17, U22, and U23 should be suspect.

Trouble inside this loop points to ICs U14, U15, U18, U19, U20, U21, U39, U40 or U45.

If new parts are substituted or exchanged for ICs U14, U15, U18, U19, U20 or U21, the converter will have to be readjusted for minimum distortion.

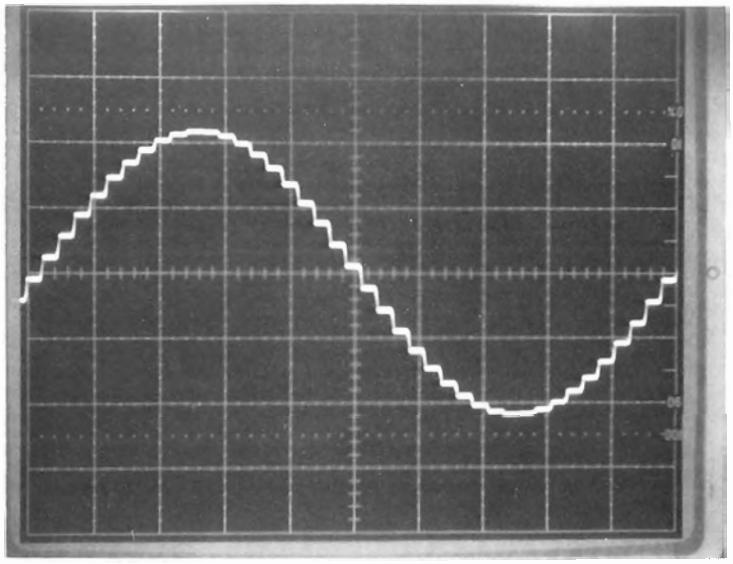


FIG. 4.4.1

Sample/Hold output (U22, pin 6) wit
1 kHz sine wave input just below
converter clipping.

Scale: Vert 2 volts/DIV
Horiz 0.1 mS/DIV

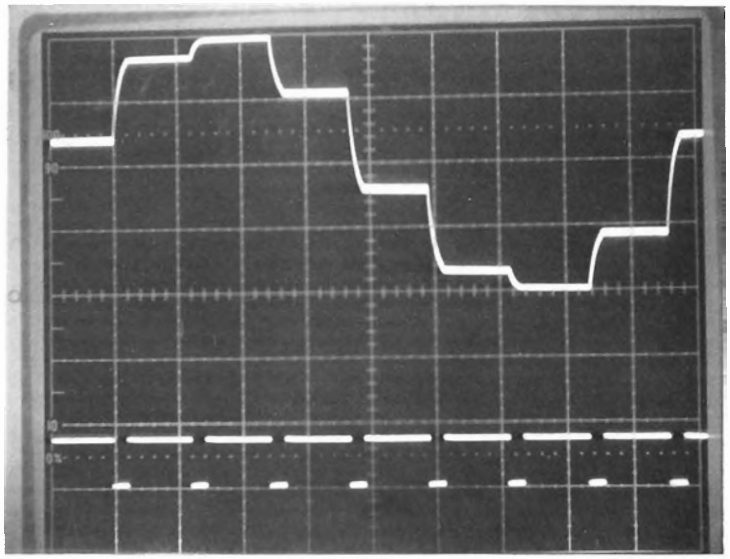


FIG. 4.4.2

Upper Trace: Sample/Hold output
(U22, pin 6) with
5 kHz sine wave input
1 dB below converter
clipping

Lower Trace: ISAM/ (U46, pin 15) w
delay multiply X1
(no modulation)

Scale: Vert 2 volts/DIV UPPER
" 5 volts/DIV LOWER
Horiz 20 µS/DIV (BOTH)

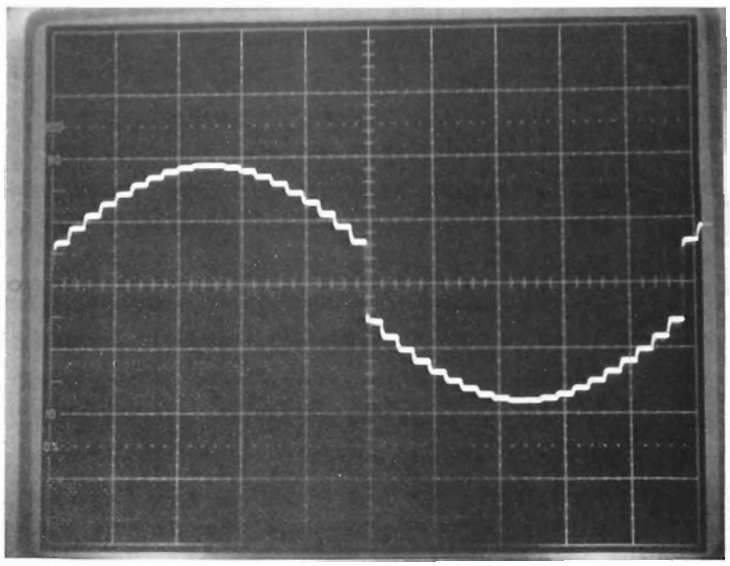


FIG. 4.4.3

Log Waveform (U21, pin 6) with
1 kHz sinewave input just below
converter clipping

Scale: Vert 2 volts/DIV
Horiz 0.1 mS/DIV

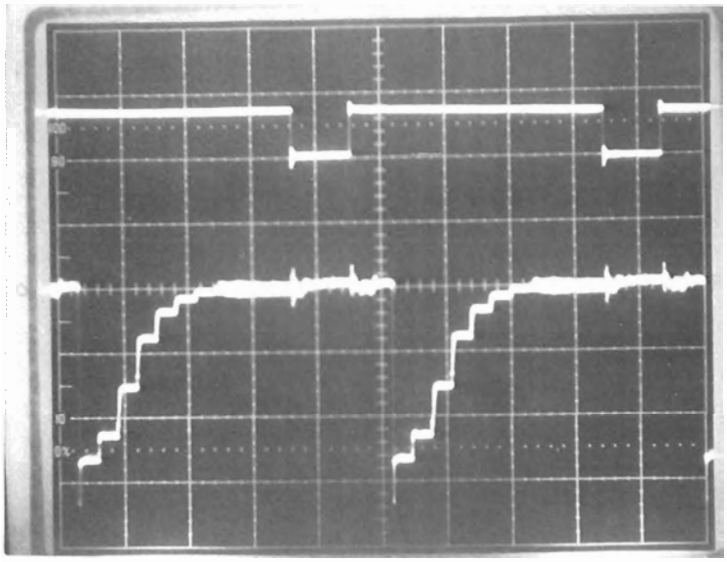


FIG. 4.4.4

Upper Trace: ISAM/ (U46, pin 15)
with delay multiply
X1 (no modulation)

Lower Trace: DAC Io/ (U20, pin 3)
with no input signal

Scale: Vert 5 volts/DIV UPPER
" 0.2 volts/DIV LOWER
Horiz 5 µS/DIV (BOTH)

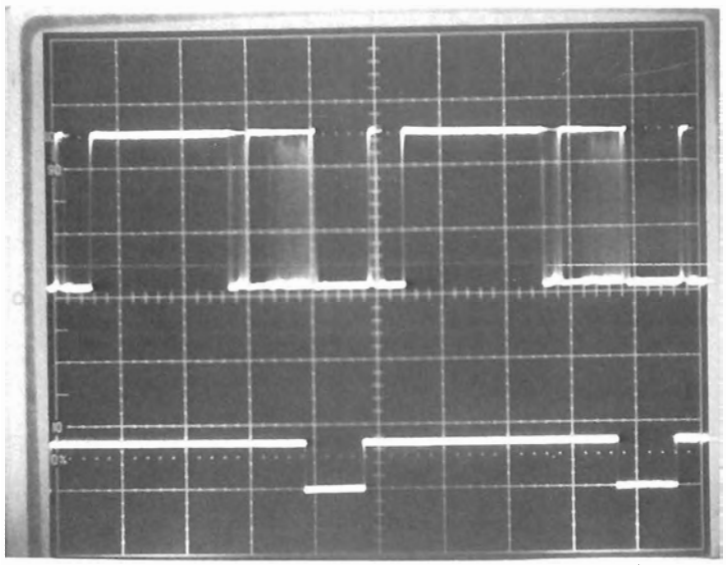


FIG. 4.4.5

Upper Trace: Comparator Data
(U20, pin 7)
with no input signal

Lower Trace: ISAM/ (U46, pin 15)

Scale: Vert 2 volts/DIV UPPER
" 5 volts/DIV LOWER
Horiz 5 µS/DIV (BOTH)

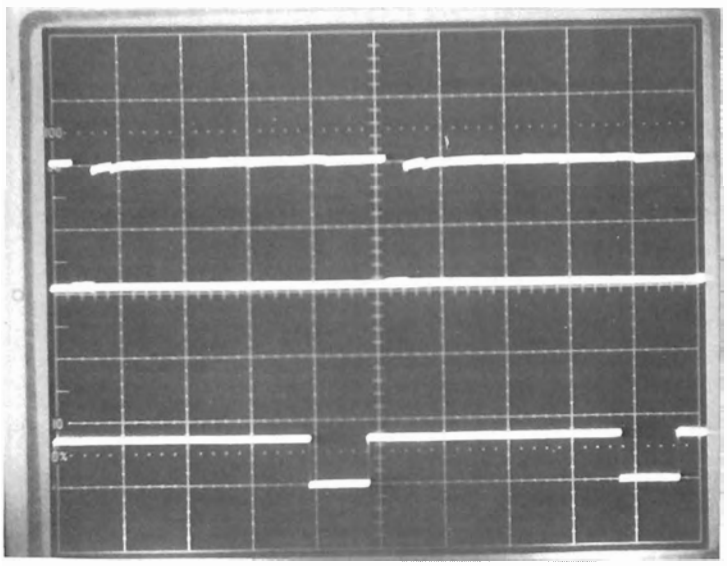


FIG. 4.4.6

Upper Trace: DAC MSB Line (U19, pin 1)
with -50 dB input signal

Lower Trace: ISAM/ (U46, pin 15)

Scale: Vert 2 volts/DIV UPPER
" 5 volts/DIV LOWER
Horiz 5 µS/DIV (BOTH)

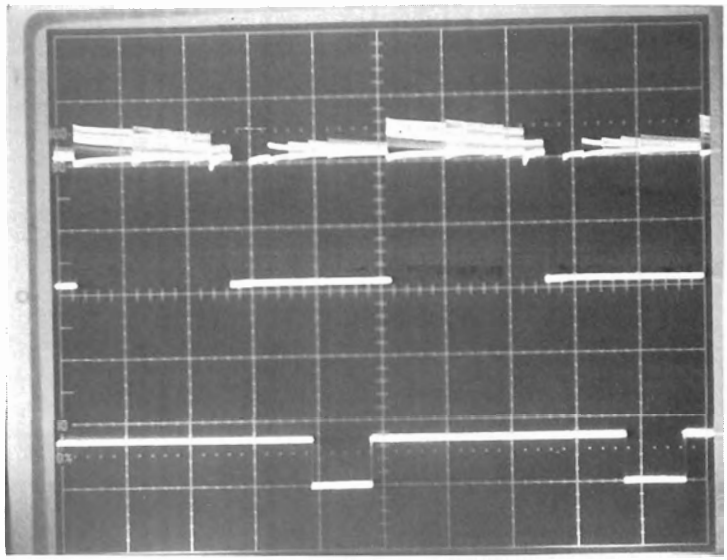


FIG. 4.4.7

Upper Trace: DAC BIT 3 line (U19, pin 9) with -50 dB input signal

Lower Trace: ISAM/ (U46, pin 15)

Scale: Vert 2 volts/DIV UPPER
" 2 volts/DIV LOWER
Horiz 5 µS/DIV (BOTH)

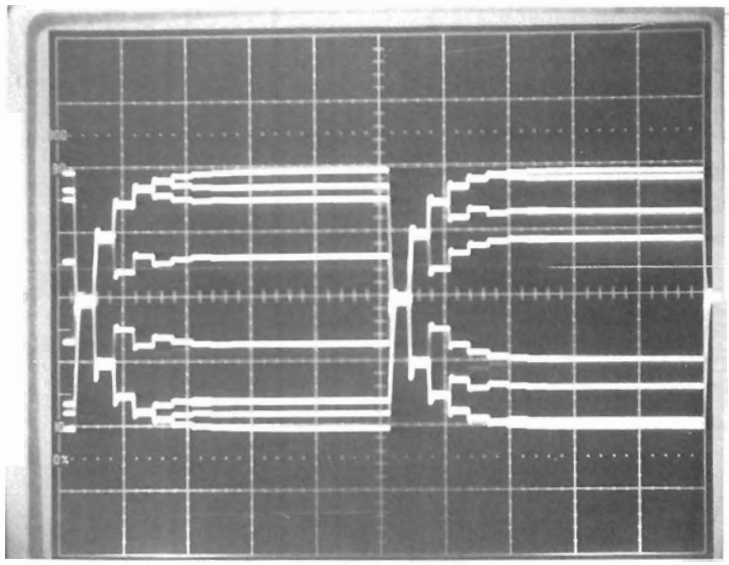


FIG. 4.4.8

D to A output voltage (U14, pin 6) with 1 kHz sine wave input 1 dB below clipping
"0" delay

Scale: Vert 2 volts/DIV
Horiz 5 µS/DIV

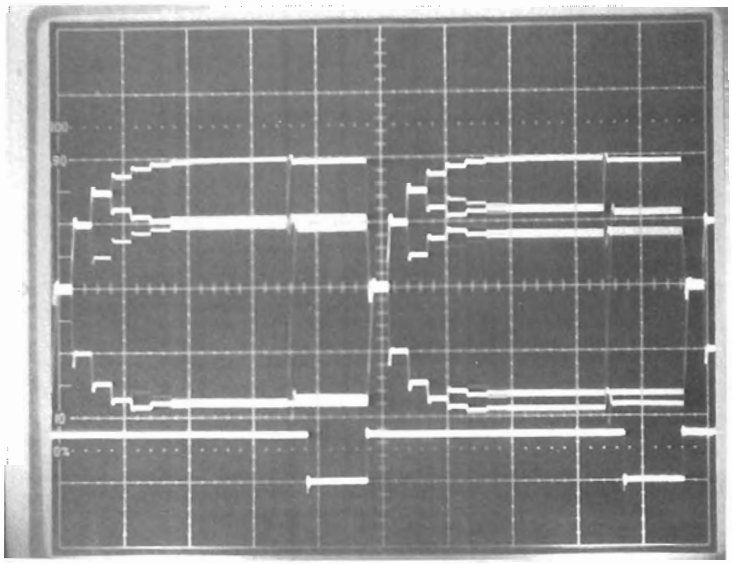


FIG. 4.4.9

Upper Trace: D to A output (U14, pin 6) with 1 kHz sine wave input 1 dB below clipping
0.8 mS delay

Lower Trace: OSAM/ (U46, pin 12)

Scale: Vert 2 volts/DIV UPPER
" 5 volts/DIV LOWER
Horiz 5 µS/DIV (BOTH)

4.5 FILTER PROBLEMS

If the problem remains when the converter has been bypassed (see section 4.4), it should next be localized to either the input or the output filter. First check the input filter by removing IC U4 and connecting a chip lead from U11 pin 7 to U4 pin 1. This allows only the input filter to appear in the input to output path of the machine.

There are two probable causes for filter malfunction: defective IC or polypropylene capacitor. Both will cause frequency response errors. A defective IC will also cause excessive distortion or noise. Try substituting ICs or, if a capacitor is suspect, bridge a 1.0 nF capacitor across each of the five filter capacitors in turn until the response returns to normal. If a filter component is replaced, recalibration may be necessary. Refer to secion 3.0.4 for a calibration procedure.

If, after calibration, you are unable to achieve satisfactory response above 10 kHz, the sample/hold, output deglitcher or aperture correction filter components may be at fault. Again, try to isolate the problem section by using the jumper technique.

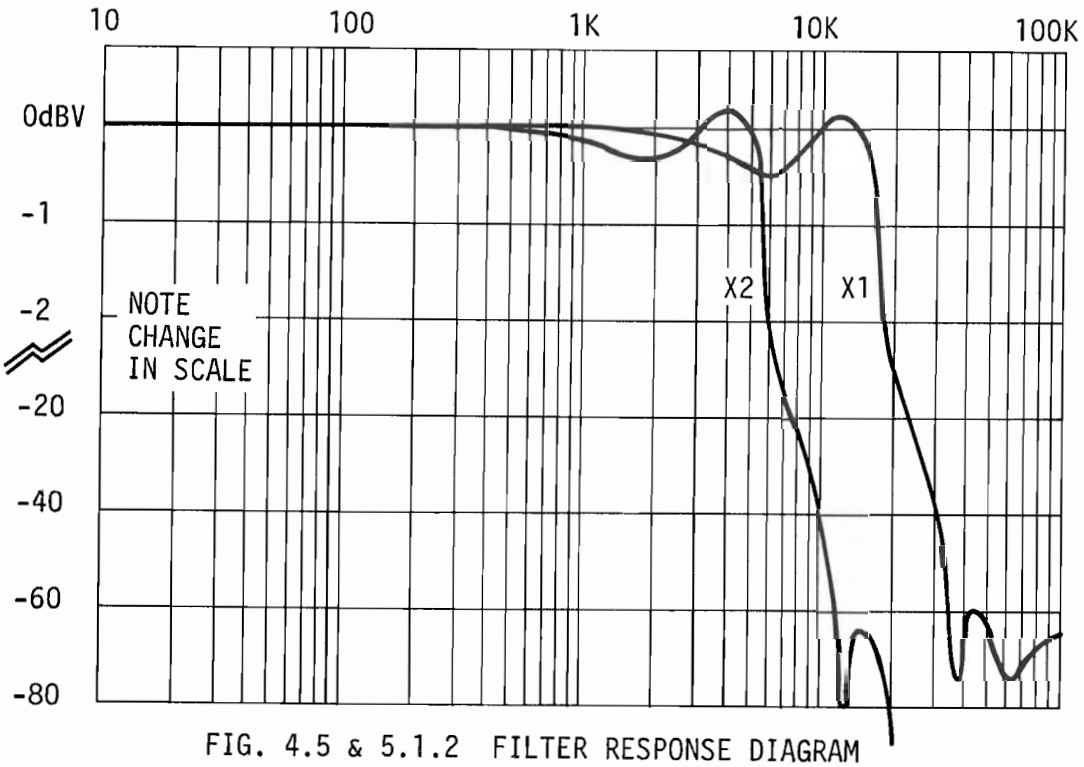


FIG. 4.5 & 5.1.2 FILTER RESPONSE DIAGRAM

4.6 SIGNATURE ANALYSIS TESTING

The PCM-41 digital logic was designed to be cost effective, simple, and testable. In general, it is possible to completely test all logic systems using a basic dual channel 20 MHz scope. An additional level of testability is also provided - Signature Analysis!

Signature Analysis, "SA", is a test method which allows a simple compact frequency counter-like instrument to display a compressed, four digit "fingerprint" of a data stream present at a node. The instrument is a "Hewlett Packard 5004A". The 5004A generates a signature from a node using a linear feedback shift register. Any fault associated with a device on a node will force a change in the data stream and therefore, result in an erroneous signature.

The actual signature is a four-character (symbol) display. Each character can be one of 16 symbols. the 16 possible characters are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, C, F, H, P, and U.

The signature has no meaning other than the fact that it is correct (expected) or incorrect. If the correct signatures are known for a digital system, then it is possible to locate and correct improper functioning sections.

In order to apply Signature Analysis the logic under test must meet several criteria:

1. The Logic must run in a repetitive loop.
2. The 5004A must know when to start looking at the data stream (START) and when to stop looking and display the signature (STOP).
3. A clock must be provided to strobe data into the 5004A (CLOCK).
4. Data and Clock must be <10 mHz.

Non-repetitive data such as an ADC output is not testable unless provisions are made to force repetitive behavior. Non-synchronous data such as a one shot output is not testable unless special provisions are made to sync the data. Analog Circuits are not generally testable.

START, STOP AND CLOCK

These functions have to be connected to the 5004A; in addition, the controlling edge has to be specified, e.g., rising or falling. Edge polarity is selected via front panel push buttons on the 5004A.

DATA

A "logic probe" like device is used to input data to the 5004A. Like conventional logic probes the 5004A's, probe has a tip light which can show presence of data, high logic levels, low logic levels, and open

or float levels. Refer to the HP 5004A Owners Manual for more details.

Since the probe is expected to accurately sense data for the 5004A to compute a signature, noise or poor wave shape will distort results. The 5004A's probe has a ground lead. Please use it to insure correct results, especially with fast logic.

TESTING THE PCM-41

In order to facilitate troubleshooting of the PCM-41, a special test connector is provided (J5), the location of this connector is between U22 and U45. The .025" square posts of this connector will mate with the CLOCK, START, STOP, and GND leads of the 5004A. The test probe is then used to sample the various logic nodes on the circuit board.

Test connector J5 also provides jumper points for substitution of signal WC1 for the SAR DATA input. This substitution forces a repetitive bit pattern causing stable signatures to be obtained from the SAR, DATA and DAC busses.

The PCM-41 Digital schematic is appended with correct signatures to facilitate test. In several instances one node may give various signatures for different delay settings etc. To present these signatures, the values are listed in a separate table (see section 6.5).

TEST PHILOSOPHY

Signature Analysis is best applied only after it is determined that a unit is not working correctly and several minutes of testing with traditional devices (scope, voltmeter, and frequency counter) has not shown a problem. If a specific problem is known, say a memory defect, then it is reasonable to go to that portion of the logic and check signatures. If little is known about the nature of the problem, then the flow chart procedure to follow should be used.

BAD SIGNATURES

If a bad signature is found one must be careful not to make quick assumptions such as "bad chip", etc. First of all it is important to work backwards though the logic structure to find where good signatures end and bad ones begin. Consider the following device, an LS374 latch with tri-state outputs.

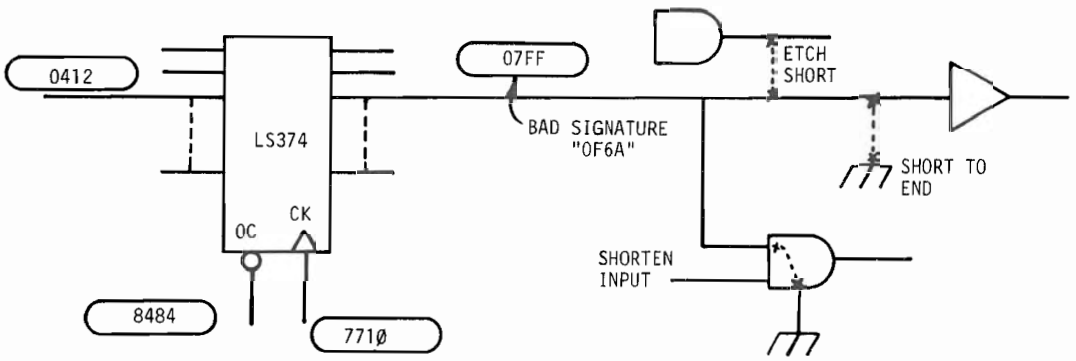


FIG. 4.6A SIGNATURE ANALYSIS EXAMPLE

If a bad signature is found, first determine if all device input signatures are good, e.g., input data, clock and output enable. If all inputs are correct and an output signature is bad, it still does not indicate a bad LS374. An output can appear bad because of etch shorts or even defective gates or flops loading the signal line. In some instances it is possible to isolate the output pin by various means (plugging in the IC with a pin bent out or removing loads) so that the suspected device can have a chance to prove itself. Once a fault is found and corrected, recheck the associated logic for good signatures.

TEST PROCEDURES

Connect the 5004A CLOCK, GND, START, and STOP inputs to the corresponding points on J5. If memory or SAR output is to be tested, remove IC U20 (removes DATA from SAR D input), and connect a jumper from J5-WC1 to J5-7. Note there are two "Z" points - use either one.

Set the START, STOP, AND CLOCK buttons as indicated on the schematic or test table being referenced. The HOLD button should be "OUT".

Use test probe to probe the various logic nodes; allow several seconds for the "Gate" lamp on the 5004A to go on and off several times.

If the "UNSTABLE SIGNATURE" lamp stays out, the signature is valid.

NOTE: Valid does not mean correct signature, it only means that the data evaluated was repetitive and the signature obtained can be compared with a known good signature.

In a number of instances the behavior of the 5004A's probe tip lamp is given in the test procedures. This probe is essentially a logic probe and can indicate logic high, low, float, and pulse activity.

If the lamp is stated to "blink" or "flash" one can assume that the lamp was either off or on and momentarily goes to the opposite state. Lamp "on" or "off" means it stays on or off. If the lamp illuminates at half intensity it means that the circuit node is open, floating, or tri-state open.

If the lamp flashes on or off it indicates either high going or low going pulses. A single narrow pulse will give a flash. For continuous pulse streams, the lamp will blink at a steady rate.

Refer to the flow chart (Fig. 4.6) for diagnostic procedures.

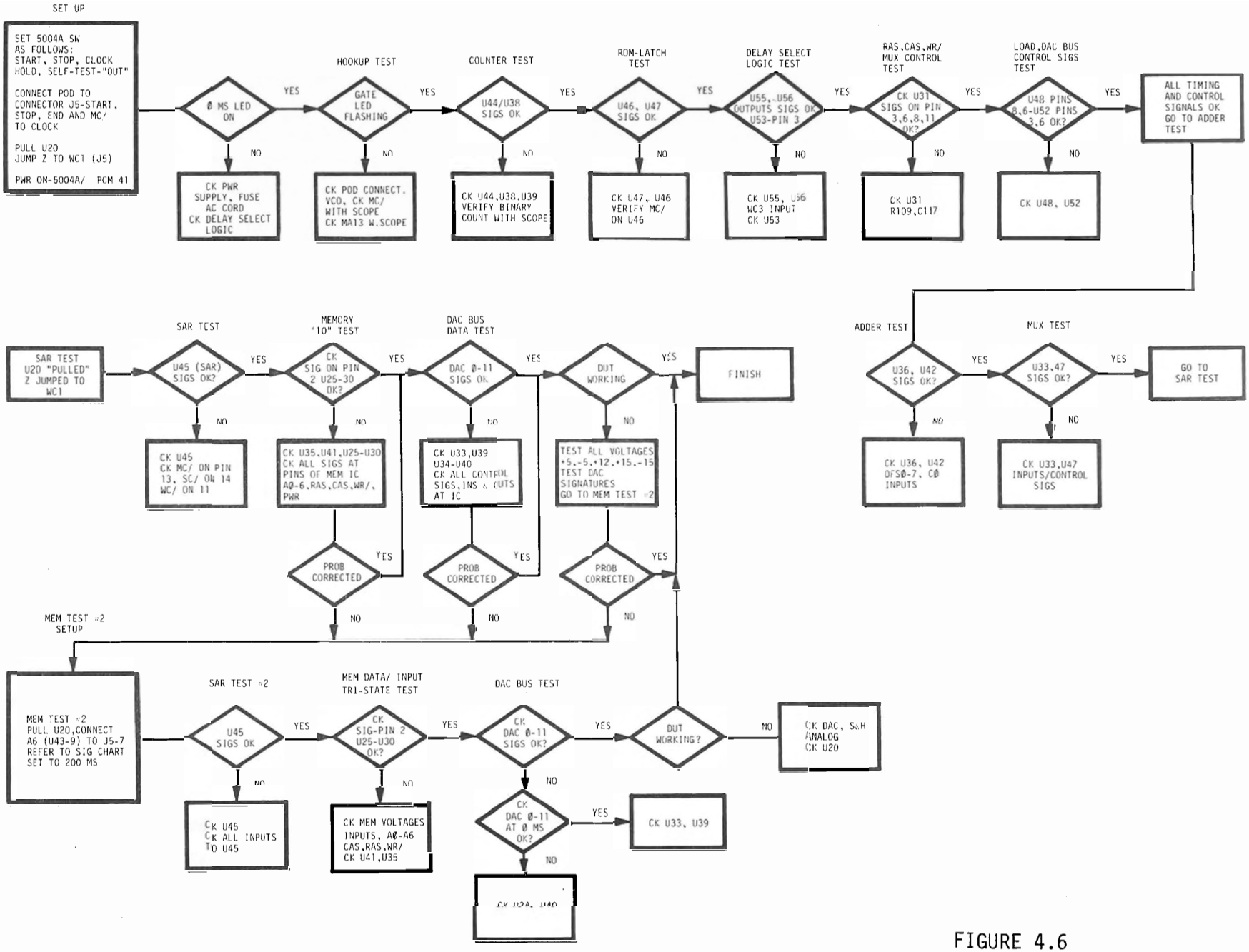


FIGURE 4.6
SIGNATURE ANALYSIS FLOW CHART

5.0 THEORY OF OPERATION

The information contained in this section has been provided as an adjunct to the troubleshooting section. It is included to provide maintenance and service personnel with a brief block-by-block circuit description of the PCM-41. It is not a primer of analog and digital circuit theory, neither is it a course on circuit design, but rather, is intended as a guide to the organization and function of the varied circuit types found within the machine.

5.1 THEORY OF OPERATION - ANALOG

The PCM-41 Analog Block Diagram is intended to provide an overall view of the analog sub-systems and their relationship to one another. The major analog subsystems are:

1. Input Section, Anti-alias Filter, Pre-emphasis
2. Input Mixer
3. Feedback Section
4. Analog to Digital Converter
5. Digital to Analog Converter
6. Output Section, Low Pass Filter, De-emphasis
7. Output Mixer, Output Buffer
8. VCO Section (see section 5.2)
9. Power Supply (see section 5.4)

This section will describe the first seven sub-systems in detail. The last two numbered sections are covered separately.

5.1.1 Input Stage

The audio signal enters the PCM-41 by way of a tip/ring/sleeve phone jack and is routed as a balanced signal to a differential input stage composed of 1/2 U10 and RP1. Here the signal is converted from balanced to single ended, low-pass filtered and limited to peaks within the op-amp input common mode range. Low pass filtering for RFI is performed by C51 and C52 with additional poles formed by RP1 and C53, C54, C55, and C56. Limiting is accomplished by diodes CR8-11 with part of RP1.

The signal is next routed to the INPUT LEVEL control R51 which has 23 dB of attenuation range and then to the second 1/2 U10 which provides 14 dB of gain or 34 dB of gain with SW2 depressed. The output of this stage is the DIRECT output signal as well as the OUTPUT MIX DIRECT signal and has an amplitude of approximately 5 volts peak at machine "0" or maximum level. Resistor R52 serves to protect the op-amp from accidental shorts at DIRECT OUT jack; CR6 and CR7 protect the op-amp from injected signals which may exceed the op-amp supply voltages; while C18 provides RFI bypassing.

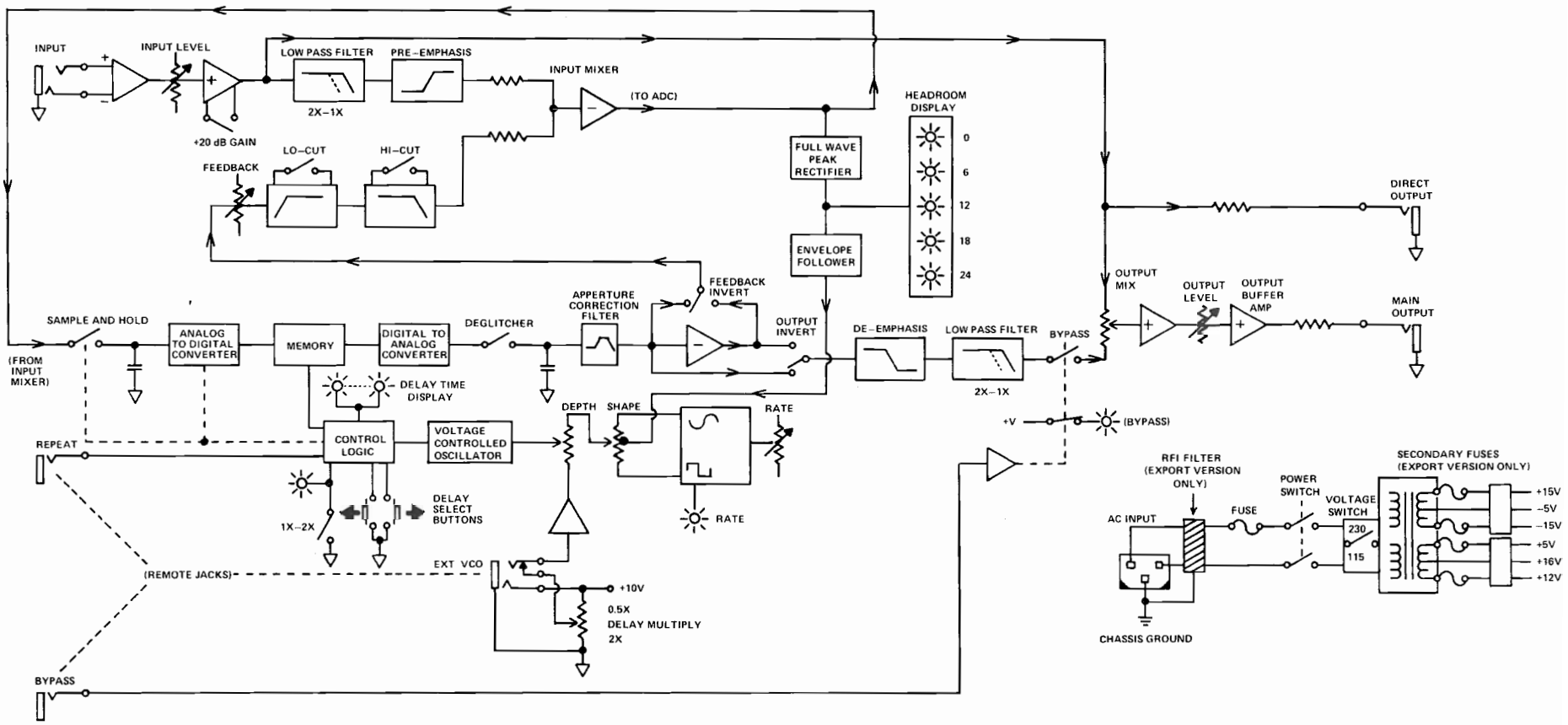


FIGURE 5.1 BLOCK DIAGRAM

5.1.2 Input Filter

The audio signal from U10 is next passed through a 5 pole eliptical low-pass filter to remove frequency components above 17 kHz from the input signal. This is called an anti-alias filter because frequency components above the Nyquist frequency (1/2 the sample frequency) of an A to D converter will be "beat down" or aliased to frequencies below the Nyquist frequency. The filter is composed of op-amps U8, U7 and 1/2 U11 as well as all associated components. While a detailed explanation of this class of filter is beyond the scope of this manual, it is helpful to refer to the figure (5.1.2) which shows the characteristic response: a pair of passband ripples and a pair of out-of-band (stopband) nulls (zeros). This particular filter response has a 0.5 dB maximum passband ripple and a 65 dB minimum stopband attenuation. The frequencies of the nulls are about 40 kHz and 62 kHz. The trimmer pots R8 and R9 are used for fine tuning the passband response of the filter. Note that the X2 switch reduces the filter cut-off frequency to approximately 6 kHz or 1/3 of the X1 cut-off frequency.

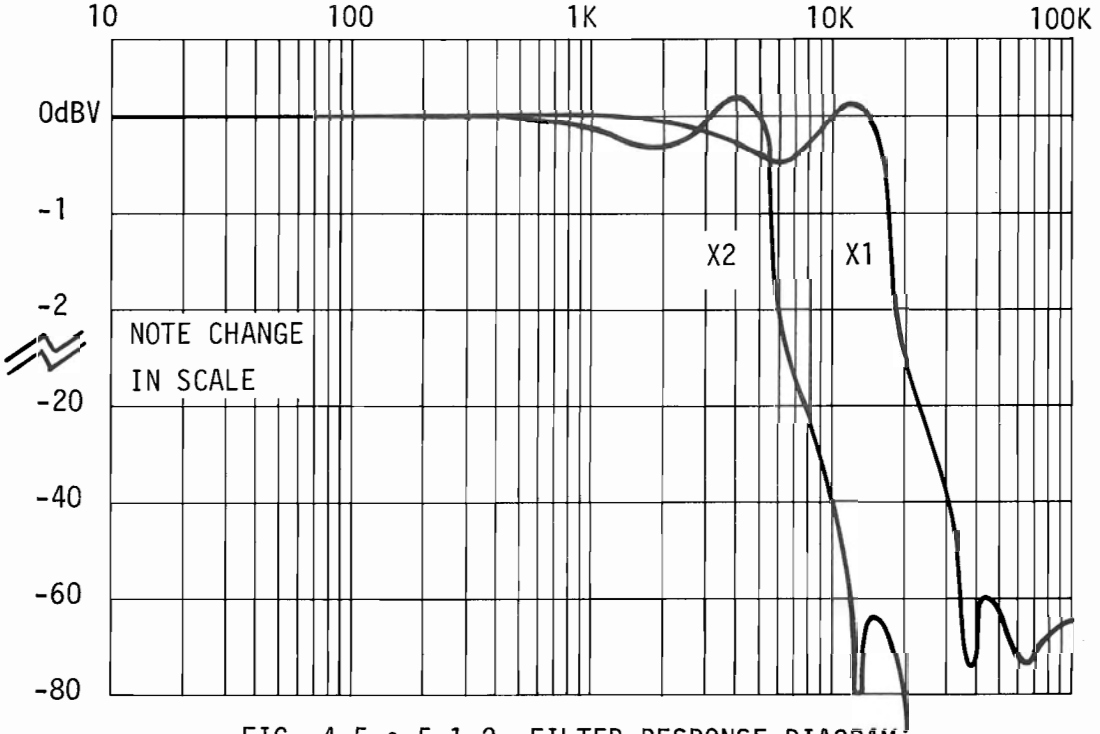
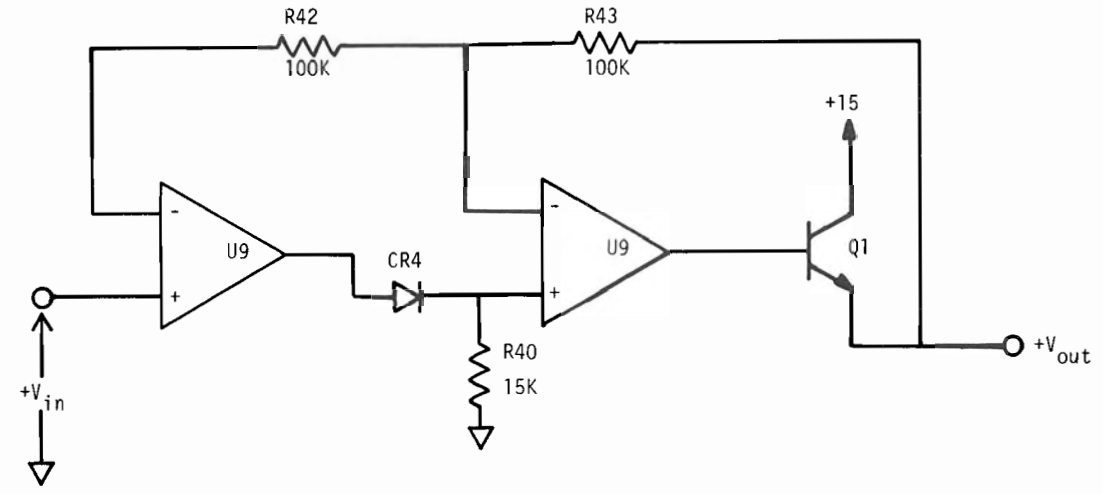
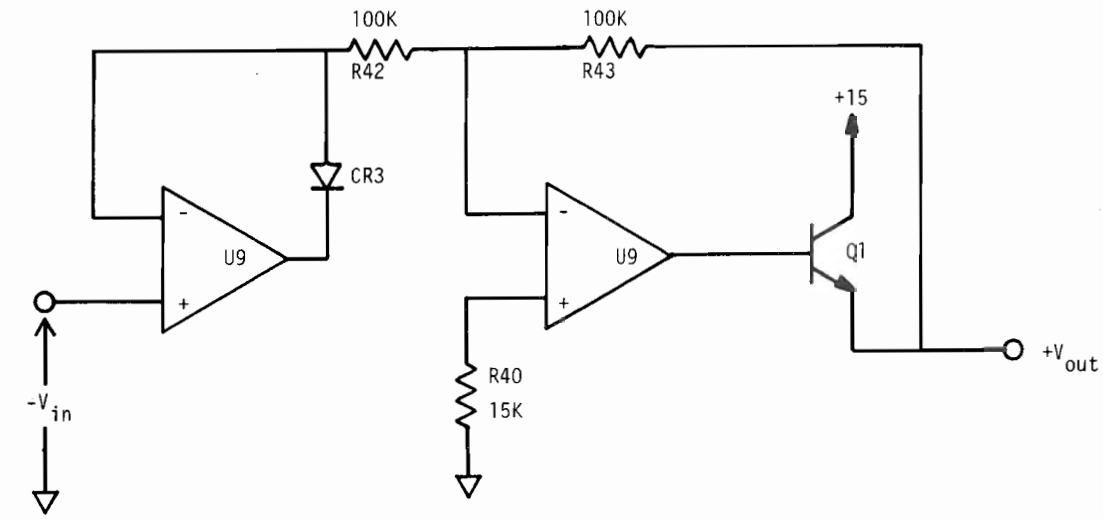


FIG. 4.5 & 5.1.2 FILTER RESPONSE DIAGRAM



FOR POSITIVE INPUTS



FOR NEGATIVE INPUTS

FIG. 5.1.4 FULL WAVE RECTIFIER

5.1.3 Pre-emphasis Network, Input Mixer

The low-pass filtered signal from U11 is next passed to the pre-emphasis network composed of R58, R59 and C60. The time constants of the network are 50 us and 12.5 us giving about 10 dB boost at 15 kHz. Resistor R61 is also connected to U11's input and serves to sum the delayed signal with the original input signal thus performing the input mix function. The output of this op-amp drives the headroom indicator and the sample/hold circuit.

5.1.4 Headroom Indicator

Since the A to D converter has a limited dynamic range, it is important to use its capabilities to the fullest. The headroom indicator helps us to do this by providing a "running" indication of the most recent peak value of the signal being converted. To do this we rectify the A.C. signal with op-amp U9, store the peak value in C31, sense this value with a series of comparators U2 and U3 set to different thresholds and use them to drive a series of LED indicators, CR52-56.

To understand the operational rectifier, refer to the figure (5.1.4) with the peak store circuit removed. Positive half cycles of the input waveform cause the output of the first half of U9 to go positive causing CR4 to conduct. This applies a positive going signal to the second half of U9 causing its output to go positive also. Since there is no current flow through R42 or R43, the output follows the input waveform satisfying the input criteria for the first half of U9. Negative half cycles of the input waveform cause the first half op-amp output to go negative causing diode CR3 to conduct. Since this op-amp now acts like a voltage follower, and the second half op-amp has its non-inverting input at ground potential (CR4 is non-conducting), this second op-amp acts as an inverting stage and its output goes positive to the same magnitude as the input waveform.

To accomplish the storage of the peak value of the waveform, an emitter follower, Q1, is incorporated inside the feedback loop of the second half of U9. This allows the capacitor C31 to be charged quickly to precisely the output value of the rectifier circuit, without the voltage drop inherent in the base-emitter junction of Q1 being subtracted from that value. C31 is discharged through R42 and R43 with a time constant dependent on the magnitude of the input signal.

The five comparators, U2 and U3, are biased at voltage levels 6 dB (2:1) apart by resistor string R12-17. The highest voltage is 4.25 volts, which is actually about 1 dB below clipping level for the A to D converter. Hysteresis for the comparators is provided by R10 and R11. This augments the "hold" characteristic of the display for better readability.

The LED's CR52-56 are connected in series and run from a constant current source (12 mA.) formed by Q2 and R45-47. The comparators progressively unshort the LED's as signal level increases. This

improves power efficiency as well as minimizing glitches in the power supply, since the power drawn by the display is constant regardless of signal level.

5.1.5 Sample/Hold

The same conditioned signal which feeds the headroom indicator is also sent to the input sample/hold. The function of this circuit is to take a fast snapshot or sample of the input signal at a precise instant in time and to hold that sample without change until the A to D converter has turned that sample into a digital "word". The sample/hold is a freeze-action device whose purpose is to freeze the value of a time varying electrical signal.

The PCM-41 sample/hold circuit is composed of IC's U22 and U23, Q4 and associated components.

In the schematic diagram (figure 5.1.5), we see that the sampling waveform, ISAM/ drives the base of Q4 low at the beginning of the track or acquistion time. The collector of Q4 goes high, turning on FET switches A, C, and D of U23. At this time switch A turns off FET switch B allowing the feedback loop, R93 and R94, to be connected to op-amp U22. U22's feedback loop also contains an integrating capacitor , C101, which is charged to the input signal value after several time constants. When signal ISAM/ goes high, Q4's collector goes low, turning off FET switches A, C, and D, thereby disconnecting the feedback resistor path. The input signal no longer can charge C101 and since U22 has an FET input stage and, hence, very low input current, the voltage charge remains in C101 and the output of U22 is held at the value it had just at the moment of switches C and D opening. The function of switch A is to turn on switch B, keeping the junction of R93 and R94 at effective ground potential. This minimizes the voltage that can be developed at the inputs of switches C and D, enabling them to be driven from a unipolar signal. Diodes CR22 and CR23 further protect U16 against input transients.

The sampling rate or frequency of the PCM-41 is nominally 40 kHz. This allows about 4.7 us for acquisition and 20.3 us for hold. The complete sampling rate range is 10 kHz to 80 kHz.

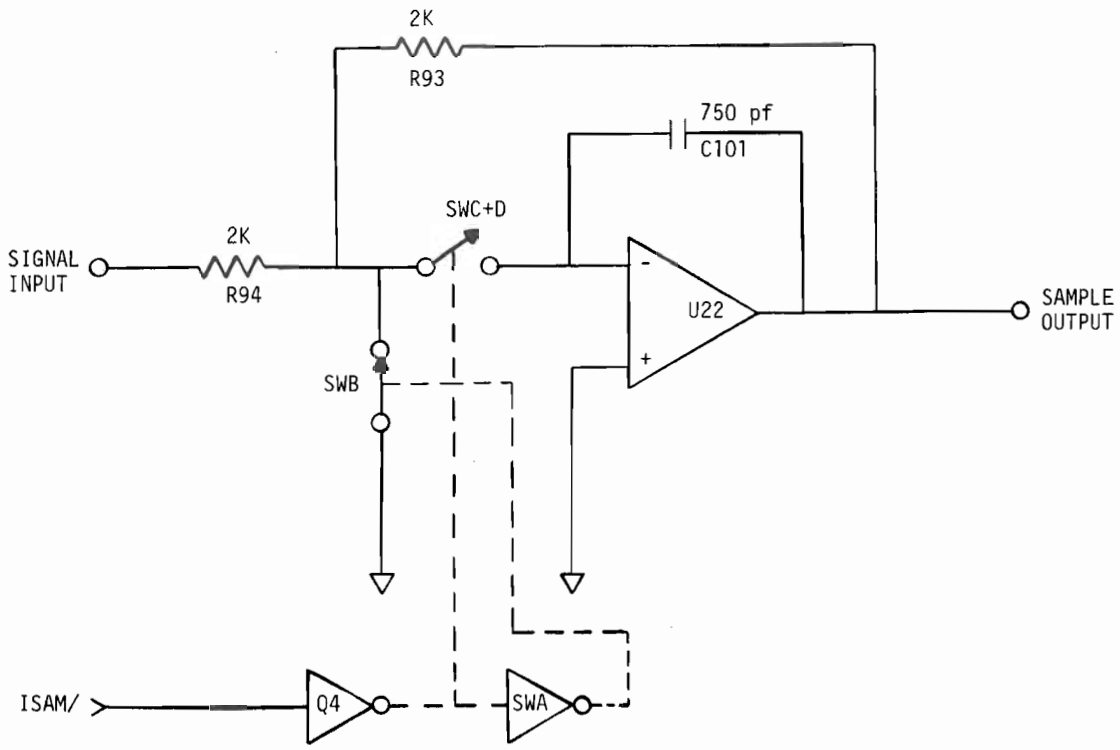


FIG. 5.1.5 SAMPLE/HOLD CIRCUIT

5.1.6 Log Circuit

The log circuit compresses the dynamic range of the sampled audio signal, enabling the A to D converter to encode a greater dynamic range. To accomplish this, resistors R87 and R90 together with op-amp U21 set the low level gain of the log circuit to approximately 15 dB. Above about 150 millivolts, the feedback path of R88, R89 and U18 begins to reduce the gain of this stage (U21) until, at 5 volts of input signal, it has slightly less than unity gain - about -2 dB. So we gain about 17 dB of dynamic range.

5.1.7 A to D Converter

The Analog to Digital converter comes next. This circuit uses IC's U19, U20 and associated components together with U45 in the digital section to form a successive approximation A to D converter. A successive approximation A to D converter, as the name implies, arrives at a digital "word" or value for the analog signal by a series of decreasing half scale approximations to the signal current.

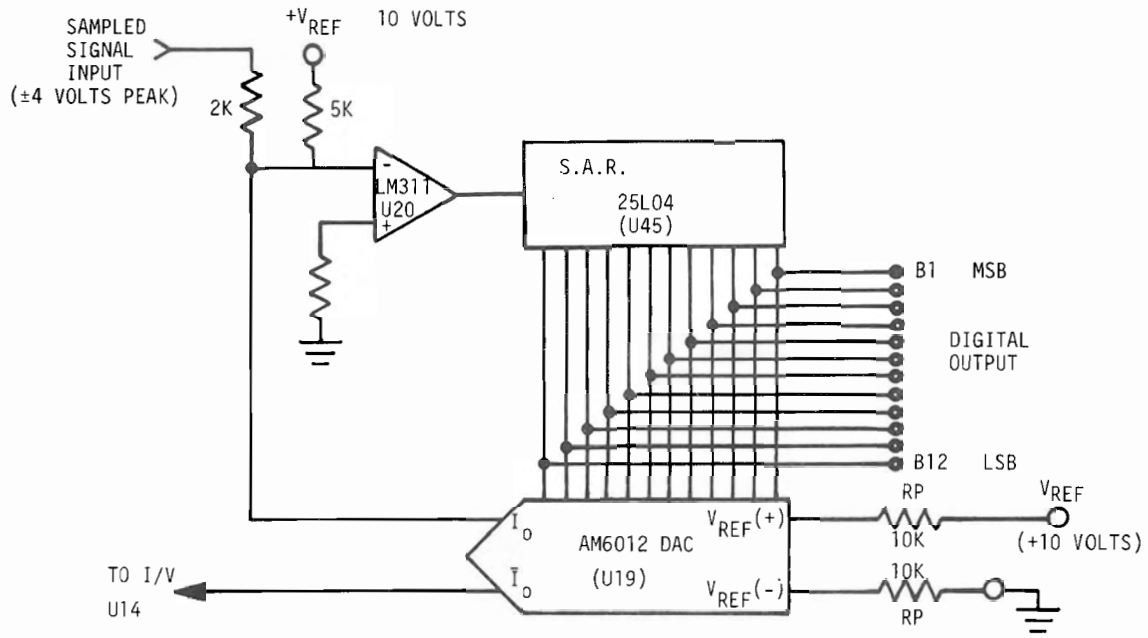


FIG. 5.1.7 A/D CONVERTER

In the PCM-41 converter, a 12-bit DAC (or digital to analog converter) is used to supply the currents for the approximations. It is made up of a series of 12 precision current sources in descending 2 to 1 steps, i.e., 2 mA. for the largest, 1 mA. for the next, 0.5 mA. the next and so on to the 12th or last which is 0.977 uA. Each current source is connected to a SPDT switch which enables it to be connected to one of two output buses (Iout or Iout/) by means of a TTL signal. (Logic 1 connects it to Iout; logic 0 connects it to Iout/.) The largest current source is called the most significant bit (MSB); the smallest, the least significant bit (LSB). There are thus 12 bit lines for U19. U19 also contains a means to program the absolute value of all the current sources together (the ratios cannot be changed.) These are the REF inputs. In the PCM-41, we program the reference current to be 2 mA for the MSB. This is derived from the +15 volt supply through resistor R68 and part of RP2. The REF inputs are op-amp inputs so the voltage at pins 14 and 15 of U19 are near zero volts, 1 mA into pin 14 gives 2 mA for the DAC MSB. The signal Iout/ from the DAC is connected to comparator U20's inverting input. Also connected there are the input signal current through R86 and part of RP2, as well as a fixed current of 2 mA through RP2. The purpose of the fixed current is to offset the bipolar signal current, thus making it unipolar. So, effectively, we have summed a unipolar, positive valued audio current with a unipolar, negative DAC current at the input of a sensitive, high-speed comparator. This comparator's output is connected to U45, a successive approximation register (SAR) which is in turn connected through 12 bit lines to the DAC's current switches.

After the sample/hold has acquired a sample of the audio signal, there is a pause while the log-circuit settles to its final value. At this instant the timing signal SC/ goes high and the conversion process begins. The SAR has switched all the current sources to Iout except the MSB which is connected to Iout/ and hence the comparator input. If the input signal plus offset current exceeds the MSB current, the comparator input will remain high (positive) and its output low. This low output (DATA) from the comparator will instruct the SAR to leave the MSB set high at the next low-to-high clock transition. At this point the next bit will be set (added to Iout/) and the comparator again will be driven high or low depending on whether the signal plus offset current exceeds or is shy of the sum of MSB plus next to MSB current (3mA). If the DAC Iout/ current now exceeds the signal plus offset current, the comparator input will be forced negative and its output go high. This will instruct the SAR to turn off the bit it has just set high and try the next bit, which is smaller still. In this way the converter approaches the value of the analog signal by halves until all 12 bits have been tried. At this time the SAR holds the 12 bit values for transfer to memory (see digital section) and another sample/hold acquisition cycle is begun.

Resistors R83 and R84 add a small amount of hysteresis to U20 to help with noise; CR18 and CR19 protect the DAC output from excess voltage.

5.1.8 D to A Converter

The same DAC used to convert analog to digital is used to return the digital "word" or information to analog form. This time the process is simpler: all the digital bits are presented to the DAC simultaneously, and after the DAC's current source switches settle, a current equal to the original analog current is available at the Iout/ port. Actually, for this operation, the Iout or complementary port is used because it eliminates the need to switch the DAC output to perform two operations. The only consequence of using this port is signal polarity inversion. Again, as in the A to D connection, an offset current is supplied by two resistors from RP2, because the DAC output current is unipolar and it is necessary to re-convert the signal to bipolar form. The DAC plus offset current is summed into the inverting input of op-amp U14 which converts it to a voltage. Again, diodes CR16 and CR17 provide excess voltage protection for the DAC.

5.1.9 Anti-Log Circuit

The voltage from the D to A converter is now re-expanded by the circuit associated with op-amp U15. This circuit is the complement of the log circuit described before. The gain for low level signals is about -15 dB and the diode elements, U18, are placed in parallel with the input resistor R73. This causes the gain of the circuit to increase for larger signals, giving about 2 dB of gain at full scale input (4 volts). In order to keep the log and anti-log circuits

matched, the diode elements for both functions are realized from a single monolithic array, U18. This ensures close initial match and temperature tracking. Slight mismatches in resistors and offsets are corrected by means of two adjustments to the converter: full scale adjustment, R82, and offset adjustment, R81. These trims are adjusted using a distortion analyzer.

5.1.10 Output Deglitcher

The signal from the anti-log circuit contains more than just the analog output. This is true because the DAC Iout port is also active during the A to D conversion, which occupies 3/4 of the sample period. The remaining 1/4 of the sample period contains the output data. The way to recover this information is to use a sample/hold circuit synchronized to the sample period. This circuit composed of 1/2 op-amp U16, switch U17 and associated components is virtually identical to the input sample/hold with the exception of C85 which is made slightly smaller to improve the settling time. The output sample switch signal is OSAM/ which occurs 1/16 sample cycle after the digital output data is switched to the DAC, to allow for settling of the anti-log circuit, and lasts for 3/16 of a sample cycle.

5.1.11 Aperture Correction Filter

The input sampling process is inherently a low-pass filter with a complex response. Analysis shows that this response can be fairly well compensated up to the Nyquist frequency by the use of a moderate 'Q' two pole low-pass filter. Op-amp U16 together with R75, R76, C82, and C83 comprise such a filter. The response of the sample/hold and the aperture correction filter are shown in figure (5.1.11).

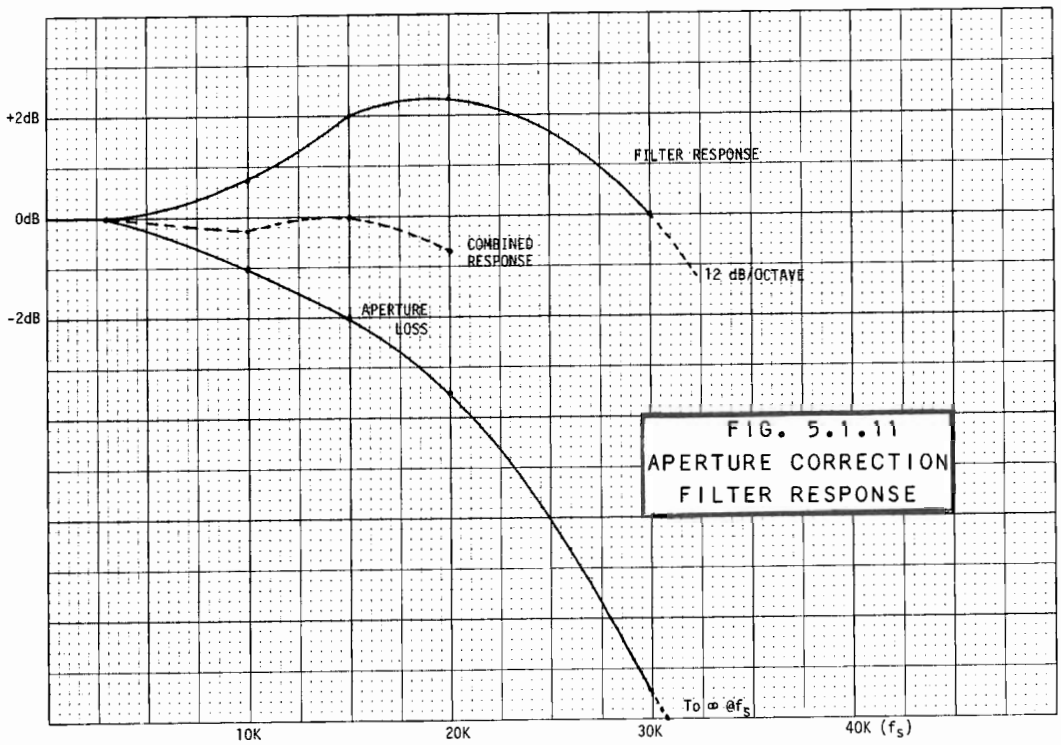


FIG. 5.1.11
APERTURE CORRECTION
FILTER RESPONSE

5.1.12 Inverter

The next circuit is a unity gain inverter (U12). It functions for both the feedback and the delay output path.

5.1.13 Feedback

The feedback circuit is composed of Feedback Level Control R54, Feedback Phase switch SW3A, Lo Filter formed by C69 with R62 and R61, and Hi Filter formed by C63 with R62 and R61. Notice that the feedback loop occurs inside the pre-emphasis/de-emphasis networks and input and output low-pass filters. This minimizes excess frequency dependent phase shifts and allows deeper nulls for flanging.

5.1.14 De-emphasis Network

Following Delay Phase switch SW4, op-amp U12 and associated components form a network whose response is the reciprocal of the pre-emphasis network's response. This network attenuates higher frequencies - above 3 kHz - and with it some of the noise generated in the conversion process.

5.1.15 Output Filter

Constructed identically to the input elliptical low-pass filter, the purpose of the output filter is to remove the sampling components from the reconstructed analog waveform. IC's involved are 1/2 U4, U5 and U6 with associated components. This filter is also switched to 6 kHz cut-off by the X2 switch.

5.1.16 Output Mixer

The output mixer allows a continuous blend of direct input signal - before filtering - with delayed signal. It is a passive mixer composed of potentiometer R100 parallelled by trimmer R99. The purpose of the trimmer is to calibrate the center detent position of the mix control for equal proportions of direct and delayed signal. FET Q3 is the bypass switch driven from Q7, a level shifter. When the FET is turned off, only direct audio remains connected to the Mix pot. Since the Mix pot's wiper is connected to a high impedance buffer, the direct signal is then passed along at unity gain regardless of the wiper position.

5.1.17 Bypass Switch

The bypass function operates by closing an external switch. In early PCM-41's, the potential at the switch was -15 volts. Connecting this

to ground through switch closure caused Q7 to conduct, pulling FET Q3 gate to -15 volts, and turning on LED CR38 through comparator U58.

In later units (from S.N. 1250 on), the potential at the switch is near +5 volts, making it compatible with the Lexicon Prime Time bypass function. In these units, the external switch directly turns on the LED CR38 and uses the comparator to invert the signal to turn off Q7. This in turn places -15 volts on the gate of FET Q3 to turn it off.

5.1.18 Output Stage

The Output Mix signal is buffered by 1/2 op-amp U4 and routed to the Output level control on the rear panel. This in turn feeds the output buffer, U1. U1 has 8 dB of gain so that system "0" levels can be boosted to maximum output. In the direct output mode, up to 42 dB of gain is available from input to main output. Again CR1 and CR2 in conjunction with R2 protect U1 from large signals accidently injected into the output. C15, 16, and 19 are for RFI filtering.

5.2 THEORY OF OPERATION - VCO AND LFO

The Voltage Controlled Oscillator or VCO may be considered the heart of this analog-digital processor. Its purpose is to provide a steady, jitter-free clock pulse by which the audio signal is converted to a digital word, stored in memory, and reconverted to analog form. The Low Frequency Oscillator or LFO generates the modulating waveforms which provide the PCM-41 with many of its signal altering effects.

5.2.1 Clock Oscillator

The master clock for the PCM-41 is generated by VCO chip U59. The frequency of oscillation is controlled by a voltage at pin 5 and a current at pin 6 together with a range setting capacitor, C141. The output at pin 3 is a square wave which must be level shifted to be TTL compatible. This is performed by Q6 and associated components. The clock frequency is 655 kHz nominal and can be varied from 352 kHz - 1.31 MHz. Resistors R122, R123 and R141 form a voltage divider which biases pin 5 of U59 and the non-inverting input of U60 to about +10 volts. U60 level shifts the VCO control voltage from the Depth pot and converts it to a current at pin 6 of U59. +10 volts from the Depth control is set by trim R141 to give 352 kHz clock frequency; 0 volts from the Depth control is set by trim R137 to give 1.31 MHz clock frequency. The supply voltage and all control pins of U59 are decoupled and carefully bypassed to avoid noise injection which would cause clock jitter.

5.2.2 Depth and Waveform Controls

The Depth (R153) and Waveform (R154) controls determine the source of modulation for the master clock oscillator. In its full CCW position, the Depth control selects an input from the Delay Multiply control or the EXT VCO input jack. In the full CW position, the Depth control selects signals from the Waveform control. Intermediate settings allow a blend of wave form modulation and manual modulation. Regardless of Depth control setting, the maximum range of voltage which can be applied to the VCO control op-amp is 0 to +10 volts.

The Waveform control selects a sine wave sweep in its CCW position, a square wave sweep in its CW position, and the Envelope follower in its detented mid position. Intermediate positions allow two effects to be blended.

5.2.3 Delay Multiply Control

The delay Multiply Control (R152) allows manual adjustment of the clock oscillator to obtain fixed delay settings intermediate to the Delay Select button settings or to provide manual delay modulation effects. This control provides a 0 to +10 volt signal to 1/2 op-amp U61 which inverts and level shifts this to a +10 volt to 0 volt signal feeding the Depth Control. (* Note: early units through S/N 1110 have this control voltage inverted). The +10 volts at the Delay

Multiply control is also available externally (through J8) to feed a foot pedal. Trim R136 sets the detented midpoint of Delay Multiply control to approximately +3 volts (+7 volts in units through S/N 1110) which corresponds to nominal clock frequency 655 kHz.

5.2.4 Envelope Follower

The Envelope follower is the rectified peak value of the conditioned input signal from the headroom indicator. This voltage is inverted, amplified, and level shifted by 1/2 of op-amp U60. The output voltage from U60 will thus be +10 volts for no input signal and 0 volts for full 0 "VU" input signal.

5.2.5 Waveform Generator

This circuit provides a low frequency sine or square wave signal with a unipolar output waveform of 0 to 10 volts. The two waveforms are generated simultaneously by the circuit consisting of 1/2 of U58, 1/2 of U61 and U62. FET input op-amp U62 is a bidirectional integrator biased at +5 volts by regulator U57. Its output is coupled to a comparator, U58, with a 10 volt hysteresis. The comparator output is inverted by U61 and used to drive the integrator through R155 and R151. Pot R155, the Rate control, sets the voltage level, and hence the current which determines the slew rate of the integrator. The integrating capacitor, C151, has additionally a pair of level dependent capacitors, C150 and C152, tied in parallel with it for a portion of its output cycle. These produce a quasi-sine wave integration slope. A portion of U58 is used to drive the RATE LED on the front panel.

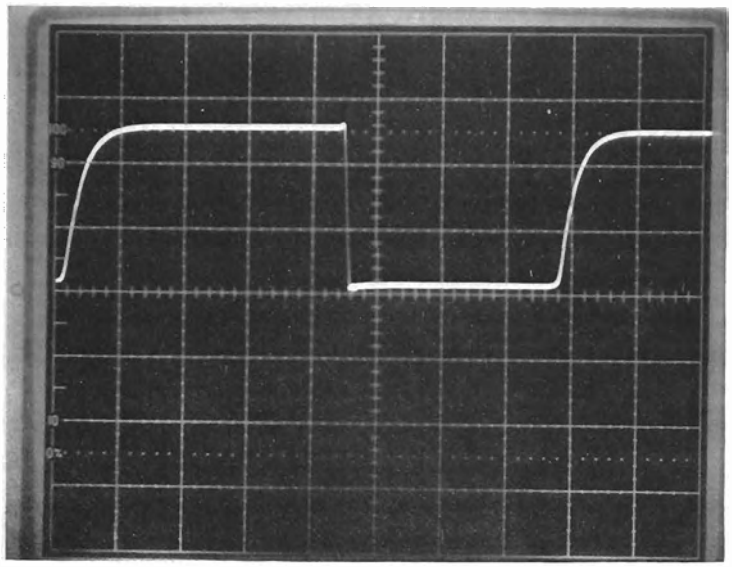


FIG. 5.2

MCØ. Delay Mult. @X1 (Collector Q6)

Scale: Vert 2 volts/DIV
Horiz 0.2 µS/DIV

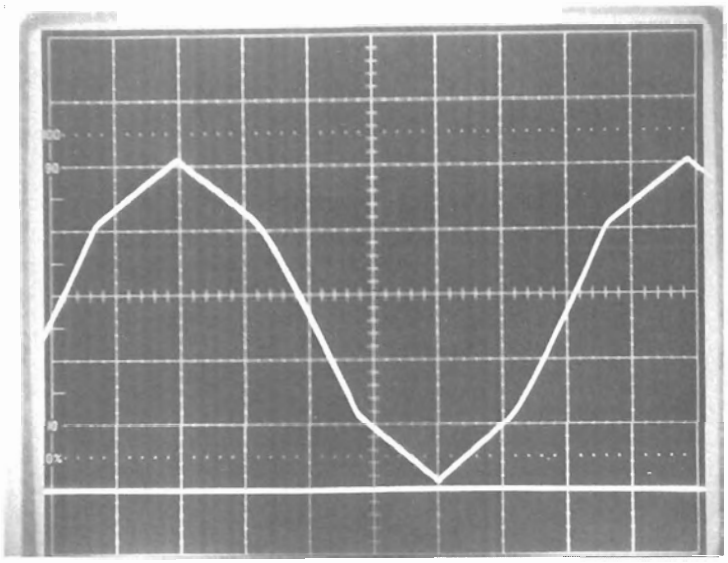


FIG. 5.2.5A

Waveform generator, L.F.O.,
(U62, pin 6)

base line = 0 volts. Rate @ 10 Hz

Scale: Vert 2 volts/DIV
Horiz 10 mS/DIV

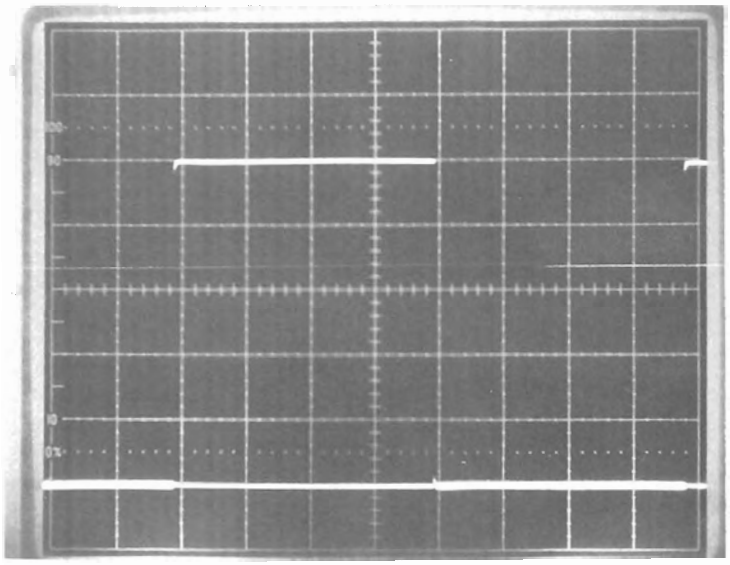


FIG. 5.2.5B

Waveform generator, L.F.O.,
(U61, pin 7)

base line = 0 volts. Rate @ 10 Hz

Scale: Vert 2 volts/DIV
Horiz 10 mS/DIV

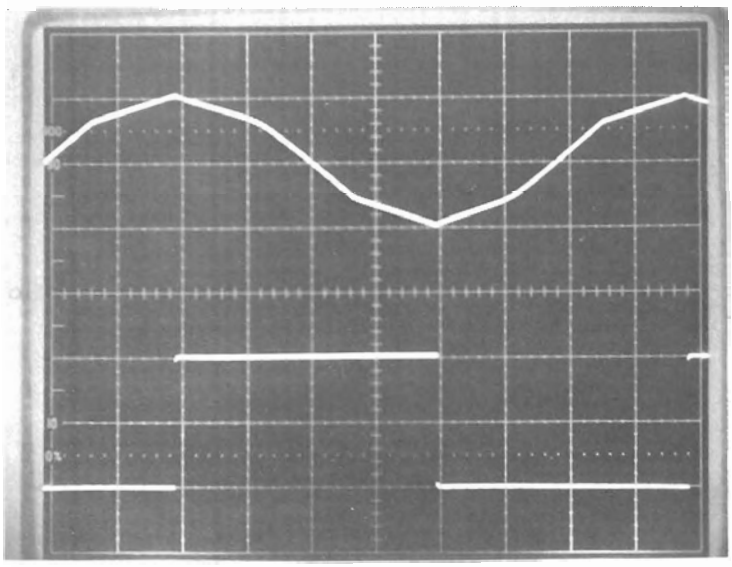


FIG. 5.2.5C

LFO showing phase relationship of
sine and square waves.

Scale: Vert 5 volts
Horiz 10 mS/DIV

5.3 DIGITAL

The PCM-41 Digital Section Block Diagram is intended to provide an overall view of the major digital subsystems and their relationship to one another in the PCM-41 Digital Section. The major subsystems are:

1. Timing Generation - (cycle counter, : 1 or 2 CTR, ROM and LATCH)
2. Address Counter
3. Delay Select Logic
4. Address Logic - (adder and multiplexer)
5. Memory - (16384 x 6 utilized as 8192 x 12 bits)
6. Bus Logic - (Databus, DAC bus, SAR bus)
7. Conversion Logic - (SAR, DAC)

Subsequent sections will detail the operation of each subsystem while the beginning of this section will contain an overview of PCM delay line operation utilizing the adder address offset technique of delay generation.

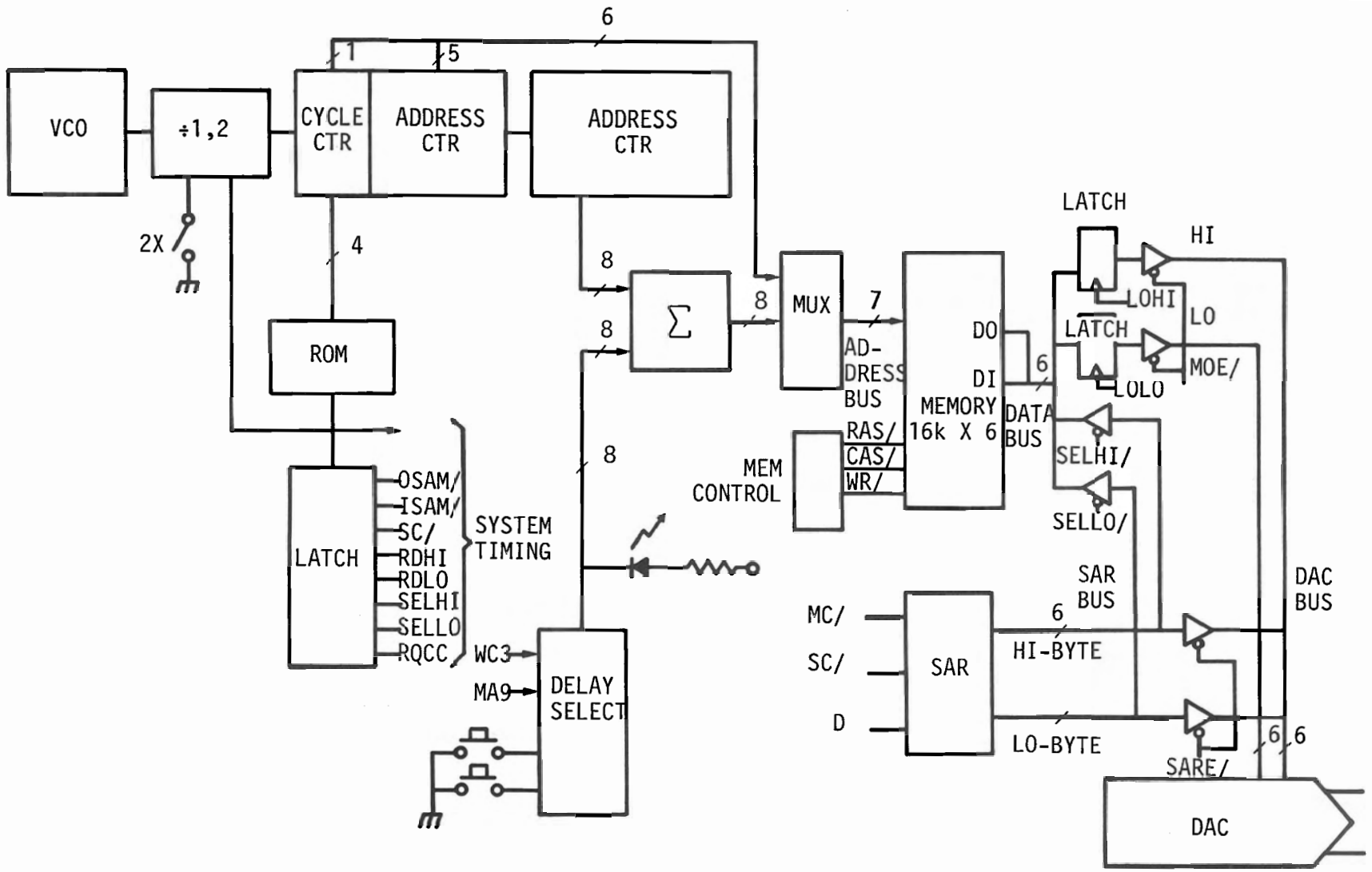


FIG. 5.3 BLOCK DIAGRAM, PCM-41 LOGIC

5.3.1 ADDRESS OFFSET LOGIC BASICS

In order to understand delay selection via address offset, it is useful to conceptualize the memory address space arranged on the circumference of a circle. Read and write address locations can be represented by a pair of points similar to the hands of a clock.

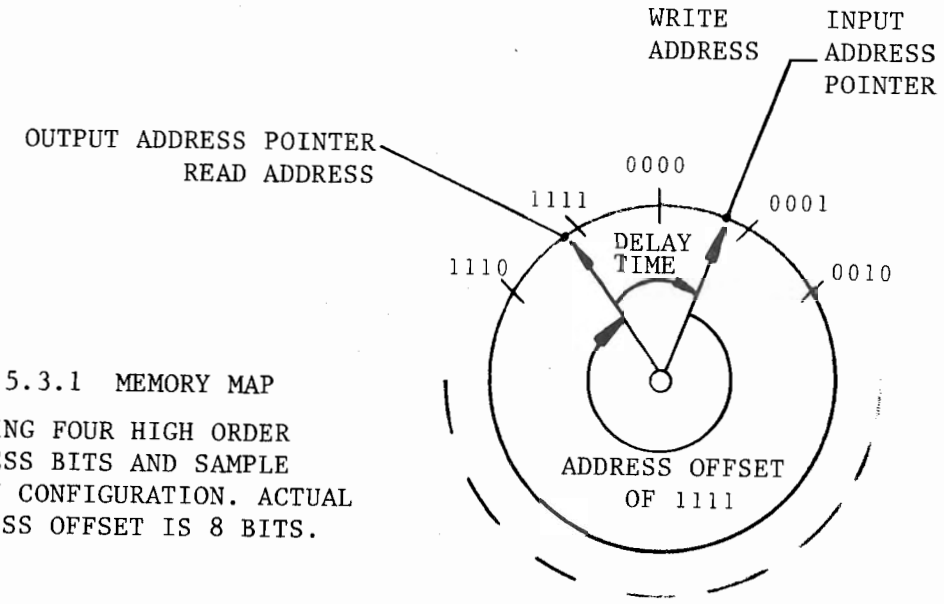


FIG. 5.3.1 MEMORY MAP SHOWING FOUR HIGH ORDER ADDRESS BITS AND SAMPLE DELAY CONFIGURATION. ACTUAL ADDRESS OFFSET IS 8 BITS.

The example given places the write pointer at the first or zero address; only 4 bits are used for simplicity. Each machine cycle data representing an analog data sample is written at the write pointer address and the pointer is advanced to the next write address.

The read pointer is thought of as trailing the write address. It advances at the same rate as the writes address reading old data. The actual displacement from the write pointer determines the delay time. The read address is computed from the write address using 74LS283 adders, U36 and U42.

The adder pair is used to add an offset to the write address. The larger the offset, the smaller the trailing distance and the shorter the time delay. For the example shown, an offset word of 1111 would position the read address one position behind the write address pointer thus producing the shortest possible time delay.

An offset of 0000 would cause the longest delay or oldest data to be read. In the actual PCM-41 logic there are 16384 address locations organized as 8192 High and Low byte storage locations. The adder is capable of adding an 8 bit offset to the 8 high order bits of the write address.

The total write address consists of 13 bits and bit WC2 which is the High-Low byte selection bit. In order to minimize parts count the addition of all ones together with a carry input bit is used rather than adding an offset of zero, e.g., adding all ones plus a carry gives the same result as adding all zeros. A word of all ones is produced by disabling decoders U55 and U56.

5.3.2 TIMING GENERATION

Refer to the Timing Diagram for specific relationships of the various timing signals used by the PCM-41.

The basic clock input to the entire PCM-41 is MCO, a signal produced by the VCO Section. The rate of MCO will vary between 352 kHz and 1.31 MHz depending on VCO setting. The nominal rate for this signal is 655 kHz (no modulation and DELAY MULTIPLY at X1).

Half of U49, a JK flip flop, is used to implement a divide by 1 or a divide by 2 counter in order to provide a 2X delay or "long delay" setting. With the 1X-2X Button in the in or 2X position, both the J and K inputs (pins 1 & 4) of U49 will be a logic "1". The flop will toggle with each falling edge of MCO. The combination of MCO and the flop output applied to AND-gate U48 will gate through every second MCO pulse producing MC/.

With the 1X-2X Button in the 1X position flop pin 4 will go to logic "0", and pin 3 of U49 will stay high allowing every MCO pulse to appear at the AND-gate output.

Half of U49 and 3 bits of counter U44 make up a 4 bit divide by 16 cycle counter. All major timing functions are generated either directly from the cycle counter bits - WC0, WC1, WC2 and WC3, or from a ROM/LATCH combination U47/U46.

ROM U47 uses WC0-WC3 as inputs; it's 8 outputs are strobed through octal latch U46 to provide glitch free timing signals. Refer to the timing chart for specific timing relationships.

The sequence of 16 states (counts) from the cycle counter comprise one complete machine word cycle. During each cycle a number of events take place; the most significant of which are:

1. An input analog data sample is converted into a 12 bit offset/binary code.

2. The 12 bit code is split into 2 six-bit bytes which are written in 2 successive write operations into memory.

3. Each of the six memories are read twice.

4. The 2-six bit words read from memory are concat-

enated to make up a 12 bit word and converted back to an analog sample.

The rate of this 16 state cycle is the sample rate. After each cycle we advance the address counter and repeat the cycle.

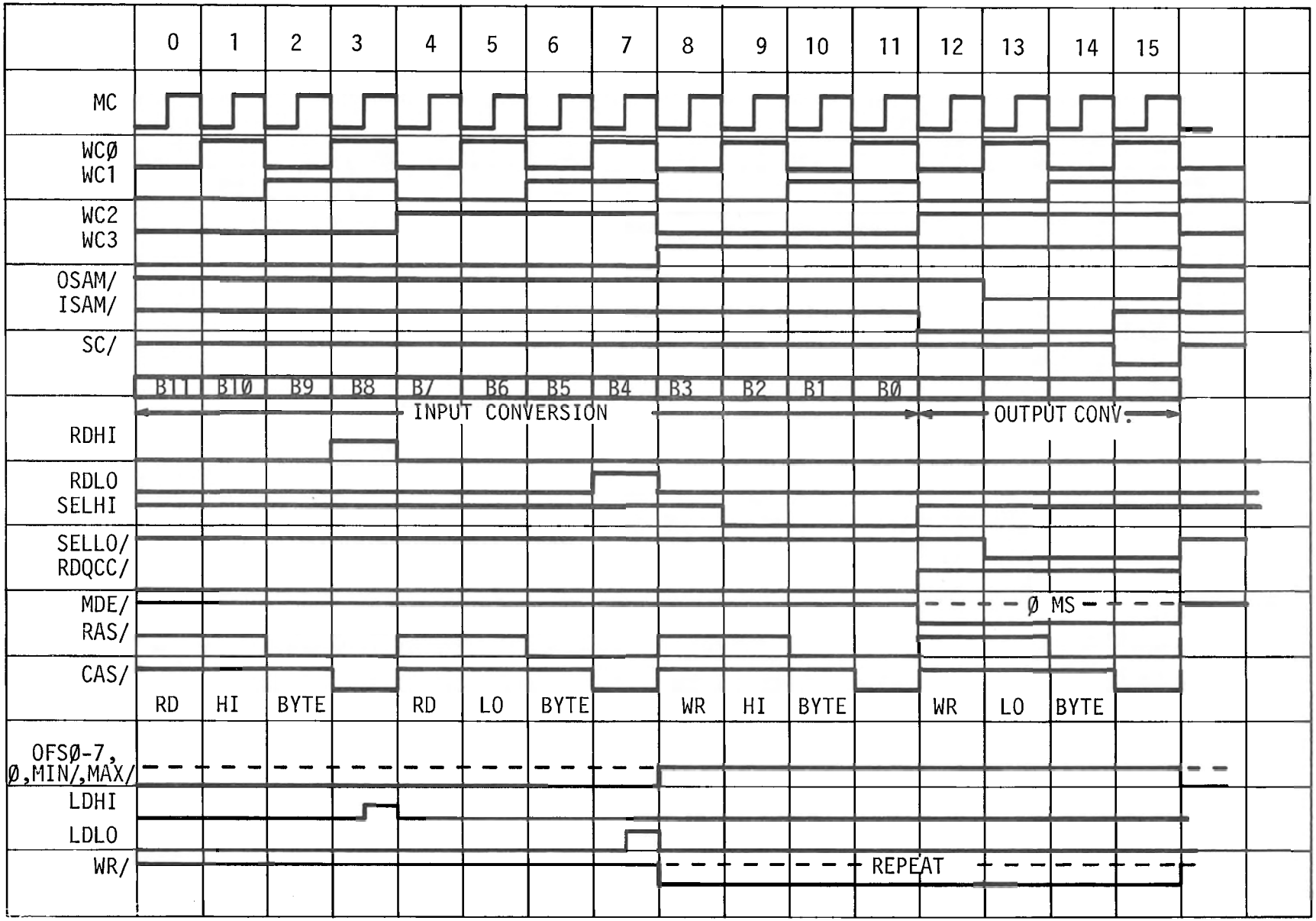


FIGURE 5.3.2 TIMING DIAGRAM

5.3.3 ADDRESS COUNTER

The Address Counter is a 13 bit binary sequence counter giving 8192 address locations. Memory is made up of six 16,384 X 1 RAMs. By assigning each 12 bit word to two successive locations (Low byte and High byte), 8192 12 bit words can be stored. The WC2 bit of the cycle counter is used for the low order address bit to memory; it is this bit which indicates high or low byte during memory read and write operations.

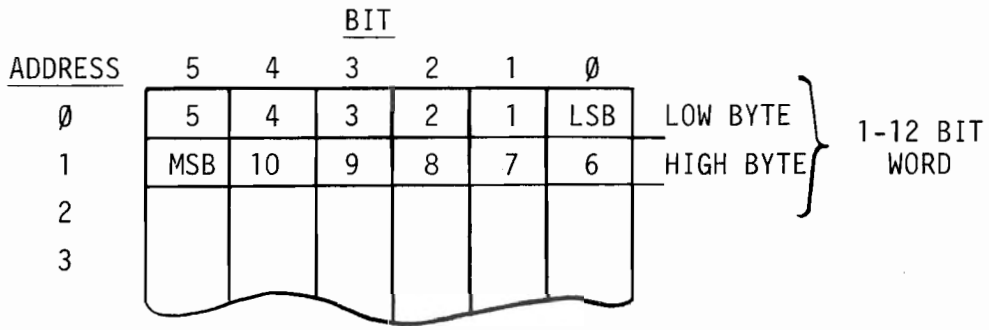


FIG. 5.3.3

FIG. 5.3.3 ADDRESS COUNTER BYTE TABLE

5.3.4 DELAY SELECT LOGIC

The Delay Select Logic consists of three parts:

1. Dual Switch Debouncer Circuits
2. Eleven-State Up/Down Counter
3. Binary to 1 of 11 State Decoder

Switch debounce is accomplished by a dual D-Type flip flop. Switch status is clocked by each flop on the leading edge of address counter bit WA9. The nominal repetition rate of this signal is every 26 ms or longer than the bounce time of the Delay Select push buttons. Both the Up and Down flops provide low signals when their corresponding buttons are pressed.

Outputs of the flops are OR'ed by U52 and differentiated by C132/U52 which produce a single clock pulse to step the Up/Down counter U54, each time either flop output goes low. Up/Down counter direction is determined by the Up-flops output which feed the steering input of the 74LS191 Up/Down counter. The 74LS191 counter is constrained to states "0" through "10" by two mechanisms.

Underflow is prevented by disabling the G (enable) input when the MIN/MAX output pin (pin 12) goes high. Pin 12 will go high only when the counter is at "0" and a down count is requested. The counter is prevented from counting up past a count of "10" (1010) by feeding the

low going decoder of this state back to the preset input of the Up-flop.

The Up-flop output is held high thus preventing further up counts. During power up sequences the counter is loaded with all zeros by a low going load pulse provided from pin 11 of U48. This load pulse goes away after 600 +/-200ms.

The Delay Select counter is decoded by a pair of 74LS138 decoders. Signal WC3 enables the decode only during the first half or read portion of a word cycle. During this enable time only one decode corresponding to the selected delay will go low. A secondary use for this low going decode is to illuminate a single LED in the Delay Time Display. The following offset words and control bits select delay taps.

DELAY(1X)	"ZERO"	"CARRY"	OFS 7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	1	1	1	1
0.8	0	0	1	1	1	1	1	1	1	1
1.6	0	0	1	1	1	1	1	1	1	0
2.4	0	0	1	1	1	1	1	1	0	1
4.0	0	0	1	1	1	1	1	0	1	1
7.0	0	0	1	1	1	1	0	1	1	1
13.0	0	0	1	1	1	0	1	1	1	1
26.0	0	0	1	1	0	1	1	1	1	1
50.0	0	0	1	0	1	1	1	1	1	1
100.0	0	0	0	1	1	1	1	1	1	1
200.0 ms	0	1	1	1	1	1	1	1	1	1

5.3.5 ADDER LOGIC

The adder inputs are the eight high order address counter bits, and eight bits plus a carry in bit (C0) from the Delay Select Logic.

Maximum delay is obtained by reading from the oldest address location (the write address). In this instance the adder sees all ones with a carry input of one added to the address counter, e.g., from a counter contents of all zeros with an offset word of all ones and a carry input of 1. The sum will be all zeros or no relative offset.

ADDRESS COUNTER	0	0	0	0	0	0	0	0	0	0	0	0	0
OFFSET	1	1	1	1	1	1	1	1					
	1	1	1	1	1	1	1	1	0	0	0	0	0
CARRY								1					
CARRY ADDRESS	0	0	0	0	0	0	0	0	0	0	0	0	0

The adders generate the write address by adding "zero" or no change to the address counter. In this instance the adder again sees all "ones" with an input carry of "one". Only in this case the source of the carry is from WC3/ OR'ed into U53.

5.3.6 ADDRESS MULTIPLEXER

The Address Multiplexer (U37 and U43) input sees a 14 bit address; using WC1 delayed and inverted as a selector it sequences the 14 bit address to the memories as 2 seven-bit bytes. The 14 bit address is made up of the following:

8 bits - Adder Outputs

5 bits - Low 5 bits of Address Counter

1 bit - Cycle Counter (High/Low Byte)

Series resistors on the multiplexer outputs act as a series line termination to limit overshoot.

5.3.7 MEMORY

Memory consists of 6-16k dynamic Random Access Memories (RAM). Each device has 3 control lines RAS/, CAS/, and WR/; a data in line, a data out line, and 7 address lines. Power required is +12, +5 and -5 volts +/-10%.

MEMORY WRITE

Address data is divided into 2 seven-bit bytes, a row address and a column address.

The first byte or row address is strobed into the memories on the falling edge of RAS/. The second byte is strobed into the memories by the falling edge of CAS/.

WR/ goes low prior to initiating the write cycles. High or Low byte is enabled by the memory by SEL HI/ or SEL LO/ signals going to U41 and U35.

The actual latching of data into memory is initiated by the falling edge of CAS/.

MEMORY READ

For Memory Read operations signal WR/ stays high. RAS/ and CAS/ falling edges strobe address row and column data into memory. Data read from memory becomes valid about 135ns after falling edge of CAS/

and remains until CAS/ returns to the high state. Data read from memory is latched in U39 or U33 determined by High of Low byte status.

It should be noted that the data-in and data-out terminals are tied together for economy of printed circuit runs.

REFRESH

Refresh occurs automatically because of the cyclic addressing inherent in this delay line application. Figure 5.3.7 shows the complete memory read write cycle.

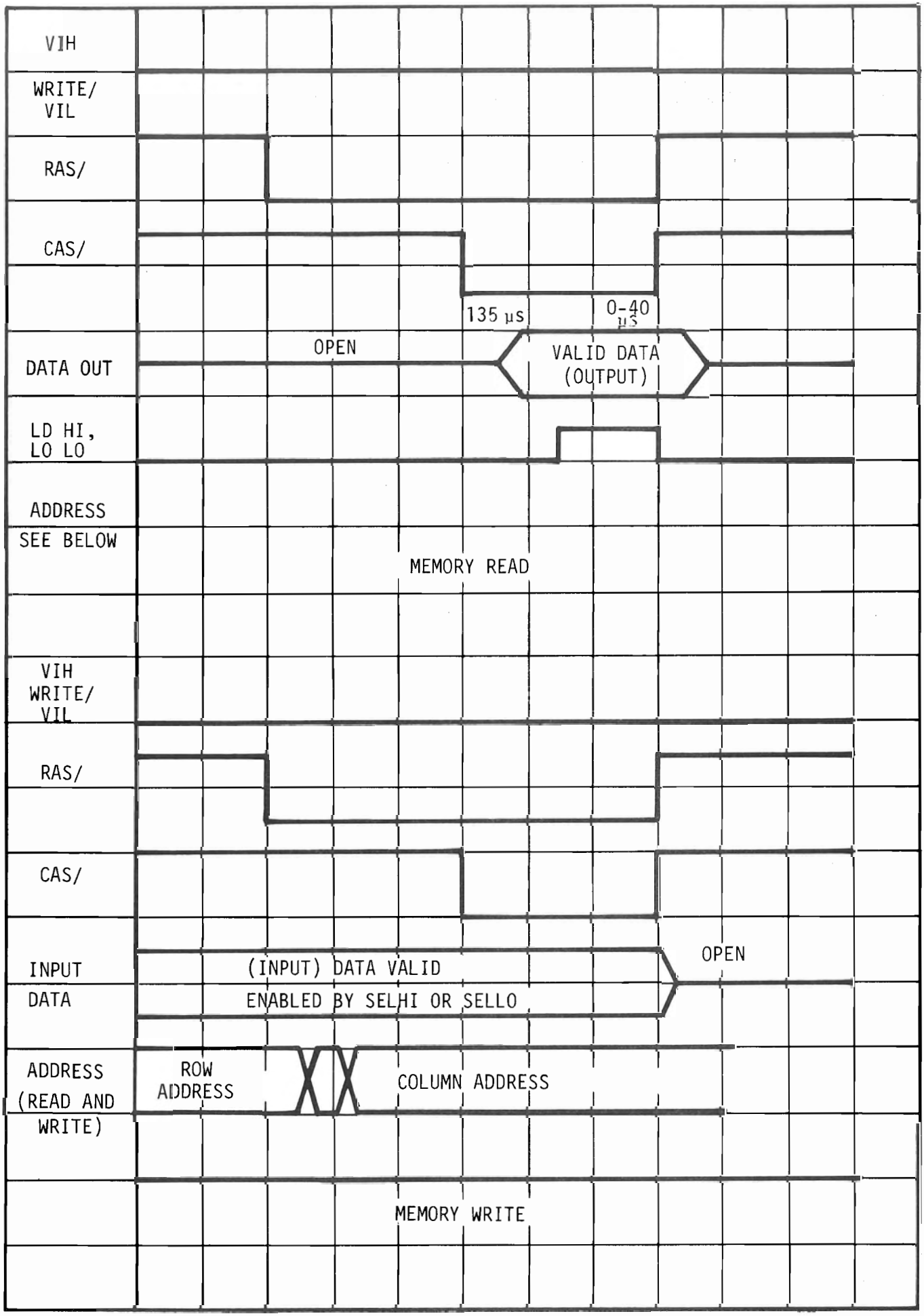


FIG. 5.3.7 MEMORY TIMING

5.3.8 BUS LOGIC

There are three bus structures used in the PCM-41 -

1. Data Bus
2. DAC Bus
3. SAR Bus

The Data Bus is a bi-directional 6 bit bus which interfaces the 6 memories to a pair of 6 bit tri-state output latches U33, U39, and a pair of tri-state input buffers U35 and U41.

The tri-state output latches take the high and low data bytes and tri-state them simultaneously onto the 12 bit DAC Bus for output conversion cycles.

The DAC Bus is also sourced by SAR data gated onto the bus by tri-state buffers U34 and U40 for output cycles of "zero-delay" audio.

The 12 bit SAR Bus sources tri-state buffers U35 and U45 which multiplex the 12 SAR bits into memory as two sequential 6 bit bytes.

Refer to the System Timing Diagram for timing relationships of bus control signals.

5.3.9 CONVERSION LOGIC

Data Conversion from analog to digital is managed by a 25L04 "successive approximation register" (SAR) U45. Conversion is initiated by negative going signal SC/ (see fig. 5.3.2). Conversion proceeds for the 12-MC clock cycles following the SC/ pulse. Conversion of the analog sample begins with the most significant data bit (MSB). The first write operation to memory occurs before completion of conversion, however, at this time, 9 bits are determined and the six most significant of the available 9 are written to memory.

SUCCESSIVE APPROXIMATION

The following diagram depicts the basic elements of the PCM-41's Analog to Digital Converter.

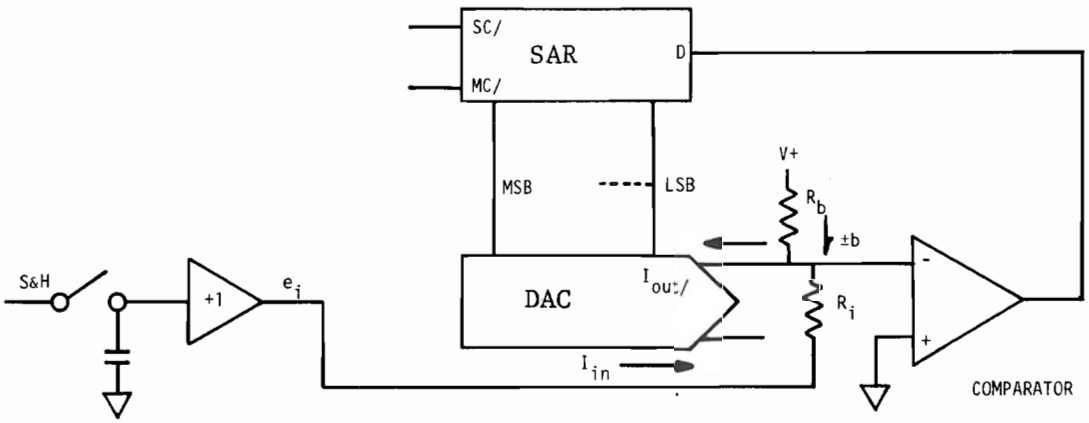


FIGURE 5.3.9 ANALOG TO DIGITAL CONVERTER

The DAC Iout/ terminal sources full scale current when all it's inputs are "0" and sources no current when all inputs are logic "1". Upon receiving the SC/ pulse the SAR will reset and output the following word:

0 11 111 111 111

This binary PCM code is the half scale value and accordingly causes the DAC to output a current equal to 1/2 its maximum value (2ma). The function of Rb is to provide an offset current equal to 1/2 of full scale. This is required because the DAC is unipolar and can only provide current values from 0 to -4 mA. A constant Ib of 2 mA shifts the output to +/-2 mA.

Assuming Ein at 0V we would have Ib balancing Id and the comparator would be somewhat fluttery with an equal probability of a one or zero output. On the other hand if Ein were say -2.5V, the comparator would output a stable logic one.

At the end of the MSB conversion cycle (assuming -2.5V input), the SAR would place the MSB at "1" (because data "D" in was logic one), and test the next bit by outputting the following word:

101 111 111 111

The DAC output will now decrease to 25% of its full scale current. Again all the currents will sum at the comparator input mode. If the comparator output is "1" the SAR will return the bit to "1" conversion, but if the comparator output is "0" the SAR will leave the bit set to "0". The process continues for 12 clock cycles. After 12 clock cycles the SAR output will be the PCM code which causes the DAC to sink a current which balances the Ib and Iin to one part/4096.

5.4 POWER SUPPLY

The power transformer has two center tapped secondaries. The first provides + and - voltages for analog circuits. These voltages are regulated by fixed 15 volt regulators U13 and U24. The negative supply is used to generate -5 volts with zener diode CR24 for the memory substrate bias.

The second center tapped winding provides +5 power through fixed regulator U64; the full unregulated voltage is available for the headroom indicator and is regulated through U63 to provide +12 volts for the memories. U63 is a programmable regulator with a floating 1.25 volt reference. This enables it to be shut off in the event of -5 volt failure. Q8 detects a short in this supply by turning on and shunting the reference pin of U63 to ground keeping its output at about +1.3 volts.

SECTION 6.0 REFERENCE

6.3.1 CHASSIS PCM-41

PART NO.	QTY.	DESCRIPTION	REF.
541-00781	4	BUMPER FEET, 3-M, SJ5025	
550-02115	4	KNOB,SKIRT,15MM,BLK,LINE,GREY,PNTER,6MM,FLAT	AUDIO SEC.
550-02116	4	KNOB,SKIRT,15MM,BLK,LINE,RED,PNTER,6MM,FLAT	VCO SEC.
550-02228	6	BUTTON, SW,WHT/BLK, SCHADOW FZ	
550-02229	1	BUTTON, SW,WHT/RED, SCHADOW FZ	PWR.SW.BUTTON
610-02269	3	HARDWARE,PC, RICHCO MB-3-156	PROT.COV. FAST.
620-01999	1	LUG,SOLDER,11/16,.020 TH,HHS #14	GRNDING LUG
630-00952	3	SPACER, SHLDER, INS., #4	REGULATORS
630-00953	4	SPACER, FIBER, #6	XFMER.MTG.
630-00953	2	SPACER, FIBER, #6	DISPLAY TO PCB
630-00891	3	INS., NYLON, #3354	J6-8
630-01853	3	INS., SILICONE RUBBER, TO-220	REGULATORS
630-02266	1	SPACER, SWAGE, BRASS, 1.125 LG,6-32 THD.	
630-02267	1	SPACER,CIR.BD., RICHCO SCBS-4N	SW.1 EXT.
630-02270	1	SPACER, PHENOLIC, 4"LG X 1/4"O.D.X	SW.1 EXT.
640-02377	14	SCREW, MACH., 4-40 X 1/4",PH,PHIL,BLK	COVERS
640-01706	2	SCREW, MACH., 4-40 X 3/8", PH	EAC301 TO CHAS.
640-01710	9	SCREW, MACH., 6-32 X 1/4", PH	PCB TO CHAS (8), DISPLAY(1)
640-01716	1	SCREW, MACH., 6-32 X 3/8", PH	DISPLAY TO PCB
640-01713	1	SCREW,MACH.,6-32 X 5/16", PH	GRND.LUG MTG.
640-02378	2	SCREW, MACH., 6-32 X 7/16",TRUSS H.,PHIL BLK	T & B COVERS
640-02288	4	SCREW, MACH., 6-32 X 1.0", PH	XFORMER MTG.
640-02271	4	SCREW, MACH., 8-32 X 3/8", FH, ALLEN,BLK	F.P. MTG.
640-02268	3	HARDWARE, BROACHING,PEM KEH 440-6	REG. MTG.
643-01733	3	NUT, 4-40, SMALL PAT.	REG. MTG.
643-01732	2	NUT, 4-40, KEP	EAC301 MTG.
643-01728	4	NUT, 6-32, KEP	XFMER MTG.
643-01728	1	NUT, 6-32, KEP	GRND.LUG MTG.
643-01734	4	NUT, 8-32, KEP	PANEL MTG.
644-01737	3	WASHER,LOCK, SPLIT, #4	REG. MTG.
644-01736	5	WASHER,FLAT, #4	EAC301 MTG.
644-01736	3	WASHER,FLAT,#4	REG.MTG.
644-01739	10	WASHER,STAR, #6	P.C.B. TO CH(8);DIS(2)
644-01739	1	WASHER, INTER.,STAR,#6	GRND.LUG MTG.
644-02379	2	WASHER,FLAT, #6 X 3/8,BLK	T&B COVERS
644-01738	3	WASHER,STAR, .690"OD X .375"ID X .031" THK.	J1-3
644-02264	1	WASHER,FLAT, BRASS,ACC.SCR 177-.125-B-7	COVER SPACER
644-02265	8	WASHER,FLAT, .296 I.D. X .375 O.D.	POTS MTG.

6.3.1 CHASSIS PCM-41 (CONT.)

PART NO.	QTY.	DESCRIPTION	REF.
701-00299	8	BRACKET, KEYSTONE #617	SUPPLIED TO CHASSIS VENDOR
701-00299	1	BRACKET, KEYSTONE, #617	DPLY PCB MTG.
700-02070	1	CHASSIS, PCM-41	
700-02072	2	COVER, PCM-41	
702-02071	1	FRONT PANEL, PCM-41	
702-02346	1	COVER,PROTECTIVE,PCM-41	
715-02197	1	ASS'Y,PC BD,MOTHER,PCM-41,PL# 020-02181	
715-02198	1	ASS'Y,PC BD,DISPLAY,PCM-41,PL#020-02185	
715-02205	1	ASS'Y,PC BD,HRI,PCM-41,PL# 020-02183	
730-02204	2	INSERT, PACKING, PCM-41	
730-02239	1	BOX, SHIPPING, PCM-41	
730-02176	1	BAG,POLY, 18" X 24" X .003", CLEAR	
070-02209	1	MANUAL, OWNERS, PCM-41	
680-00841	1	CORD, POWER, PHILIPS, 13E37-1	

6.3.2 MOTHERBOARD

PART NO.	QTY.	DESCRIPTION	REV.
RESISTORS			
200-02107	4	RES.,VAR., RTY,PC, 10K,LINEAR	R1,51,54,153
200-02108	3	RES.,VAR., RTY,PC, 10K,LINEAR,DTENT,CT	R100,152,154
200-02109	1	RES.,VAR., RTY,PC, 500K,LOG.	R155
201-00429	5	RES.,TRM., ST,PC, 2K,SA,CC,PT10V	R6-9,136
201-00438	1	RES.,TRM., ST,PC, 25K,SA,CC,PT10V	R99
201-00439	4	RES.,TRM., ST,PC, 25K,SA,CER,72PR25K	R81,82,137,141
202-00505	1	RES.,CF, 5%,1/4W, 10 OHM	R83
202-00514	4	RES.,CF, 5%,1/4W, 100 OHM	R2,106-108
202-00515	1	RES.,CF, 5%,1/4W, 150 OHM	R48
202-00517	3	RES.,CF, 5%,1/4W, 200 OHM	R45,119,120
202-00522	1	RES.,CF, 5%,1/4W, 360 OHM	R17
202-00523	1	RES.,CF, 5%,1/4W, 390 OHM	R16
202-01077	1	RES.,CF, 5%,1/4W, 560 OHM	R52
202-01228	1	RES.,CF, 5%,1/4W, 620 OHM	R55
202-00527	1	RES.,CF, 5%,1/4W, 750 OHM	R15
202-00529	4	RES.,CF, 5%,1/4W, 1K OHM	R49,85,109,111
202-00531	5	RES.,CF, 5%,1/4W, 1.5K	R14,44,113,134,135
202-00537	1	RES.,CF, 5%,1/4W, 3.0K	R13
202-00538	13	RES.,CF, 5%,1/4W, 3.3K	R3,46,50,79,80, R95,96,102-105,110,115
202-00543	3	RES.,CF, 5%,1/4W, 5.1K	R121,133,150
202-00546	1	RES.,CF, 5%,1/4W, 7.5K	R56
202-00549	12	RES.,CF, 5%,1/4W, 10K	R5,53,63,64,114,146, R116-118,132,140,149
202-01225	1	RES.,CF, 5%,1/4W, 6.2K	R4
202-00553	9	RES.,CF, 5%,1/4W, 15K	R11,12,40,41,47, R129-131,148
202-00559	5	RES.,CF, 5%,1/4W, 30K	R57,98,112,138,139
202-00561	1	RES.,CF, 5%,1/4W, 36K	R147
202-00569	2	RES.,CF, 5%,1/4W, 91K	R128,158
202-00570	6	RES.,CF, 5%,1/4W, 100K	R42,43,84,91,92,159
202-00572	1	RES.,CF, 5%,1/4W, 120K	R151
202-00576	1	RES.,CF, 5%,1/4W, 200K	R127
202-00577	1	RES.,CF, 5%,1/4W, 300K	R126
202-00580	1	RES.,CF, 5%,1/4W, 1MEG	R97
202-01497	1	RES.,CF, 5%,1/4W, 2MEG	R10
202-00503	1	RES.,CF, 5%,1/2W, 1.5K	R101
203-01489	1	RES.,MF,RN55, 1%,1/8W, 499 OHM	R157
203-02289	2	RES.,MF,RN55, 1%,1/8W, 562 OHM	R19,30
203-00456	1	RES.,MF,RN55, 1%,1/8W, 1.00K	R68
203-02290	2	RES.,MF,RN55, 1%,1/8W, 1.21K	R24,35
203-00459	7	RES.,MF,RN55, 1%,1/8W, 2.00K	R69,77,78,93,94, R123,124
203-01460	1	RES.,MF,RN55, 1%,1/8W, 2.05K	R86
203-01137	1	RES.,MF,RN55, 1%,1/8W, 4.12K	R156
203-00464	14	RES.,MF,RN55, 1%,1/8W, 4.99K	R22,23,25,26,33, R34,36,37,70,71, R88,89,122,145

6.3.2 MOTHERBOARD (CONT.)

PART NO.	QTY.	DESCRIPTION	REF.
RESISTORS CON'T			
203-02291	4	RES.,MF,RN55, 1%,1/8W, 5.49K	R18,29,58,67
203-01251	4	RES.,MF,RN55, 1%,1/8W, 8.06K	R74-76,90
203-01162	2	RES.,MF,RN55, 1%,1/8W, 9.31K	R61,62
203-00471	2	RES.,MF,RN55, 1%,1/8W, 10.0K	R21,32
203-00475	2	RES.,MF,RN55, 1%,1/8W, 11.5K	R27,38
203-00476	2	RES.,MF,RN55, 1%,1/8W, 12.1K	R28,39
203-00478	2	RES.,MF,RN55, 1%,1/8W, 13.7K	R20,31
203-01246	4	RES.,MF,RN55, 1%,1/8W, 17.4K	R59,60,65,66
203-00487	1	RES.,MF,RN55, 1%,1/8W, 30.1K	R144
203-01671	2	RES.,MF,RN55, 1%,1/8W, 47.5K	R73,87
203-00489	2	RES.,MF,RN55, 1%,1/8W, 71.5K	R142,143
203-01145	1	RES.,MF,RN55, 1%,1/8W, 1.24MEG	R72
205-01155	1	RES.,NET,DIP, 2%,1/8W, 68 OHM X 7	RP3
205-01133	2	RES.,NET,DIP, 1%,1/8W, 10K X 8	RP1,2
CAPACITORS			
240-00611	8	CAP.,ELECT.,RAD,16V, 22UF	C1,2,71,72,92,93, C129,136
240-00614	2	CAP.,ELECT.,RAD,16V, 47UF	C160,161
240-00617	1	CAP.,ELECT.,RAD,16V, 470UF	C158
240-00622	1	CAP.,ELECT.,AXIAL,16V, 4700UF	C157
240-00613	5	CAP.,ELECT.,RAD,25V, 22UF	C74,75,88,89,143
240-01262	1	CAP.,ELECT.,RAD,25V, 330UF	C14
240-02284	2	CAP.,ELECT.,AXIAL,35V, 1000UF	C94,106
240-00608	1	CAP.,ELECT.,RAD, 50V, 2.2UF	C31
241-00652	1	CAP.,TANT,RAD,25V.,4.7UF	C162
244-00660	1	CAP.,MYLAR,RAD, 10/10,100V, .01UF	C90
244-00662	4	CAP.,MYLAR,RAD, 5/5,250V, .1UF	C69,150-152
244-01488	1	CAP.,POLYCARB,RAD,10/10,100V, .22UF	C142
244-02104	5	CAP.,POLYPRO,AXIAL, 2.5/2.5,160V, 100PF	C53-56,141
244-01166	2	CAP.,POLYPRO,AXIAL, 2.5/2.5,160V, 240PF	C83,85
244-01167	1	CAP.,POLYPRO,AXIAL, 2.5/2.5,160V, 750PF	C101
244-01151	10	CAP.,POLYPRO,AXIAL, 2.5/2.5,160V, 1000PF	C4,6,8,10,12,22, C24,26,28,30
244-01169	14	CAP.,POLYPRO,AXIAL, 2.5/2.5,160V, 2200PF	C3,5,7,9,11,21,23,25, C27,29,60.62,68,82
244-01172	1	CAP.,POLYPRO,AXIAL, 2.5/2.5,160V, 6800PF	C63
245-02105	3	CAP.,CER.,RAD, 10/10,500V, 5PF	C78-79,98
245-01164	14	CAP.,CER.,RAD, 10/10,500V, 10PF	C34-37,40-43,47, C48,59,61,66,67
245-00590	11	CAP.,CER.,RAD, 10/10,500V, 150PF	C15,16,18,19,46, C51,52,70,103,117,132
245-00594	3	CAP.,CER.,RAD, 10/10,500V, .001UF	C138,140,149
245-00596	2	CAP.,CER,.RAD, 20/20,1.6KV, .005UF	C163,164

6.3.2 MOTHERBOARD (CONT.)

PART NO.	QTY.	DESCRIPTION	REF.
CAPACITORS CON'T			
245-00600	56	CAP.,CER.,RAD, 80/20,35V, .02UF	C13,17,20,32,33, C38,39,44,45,49, C50,57,58,64,65, C76,77,80,81,84, C86,91,97,99,100, C102,105,107,108, C115,116,118-125, C127,128,130,131, C133-135,137,139, C144,146-148,153-156
245-01651	14	CAP.,CER.,RAD, 80/20,50V, .1UF	C109-114,126,145, C73,87,95,96,104 C109-114,126,145, C159
270-00779	2	IND. BEAD FERRITE	FB1,2
DIODES			
300-01029	31	DIODE, SIL, 1N4148	CR1-11,16-19,21-23,25-27 CR25-37
300-01030	14	DIODE, SIL, 1N4004	CR12-15,40-43,46-51
300-01154	1	DIDOE, 1N751 ZENER	CR24
300-01032	2	DIODE, 1N5404	CR44,45
300-02401	1	DIODE, SCHOTTKY, BAR35	CR20
TRANSISTORS			
310-01009	2	XSISTOR, FET, J113-18(2N4393)	Q3,8
310-01003	3	XSISTOR, MPS 2369	Q4-6
310-01007	1	XSISTOR, 2N3904	Q1
310-01237	1	XSISTOR, MJE170	Q2
310-01008	1	XSISTOR, 2N3906	Q7
INTEGRATED CIRCUITS			
330-00692	3	IC, DIGITAL, 74LS00	U31,52,53
330-00696	1	IC, DIGITAL, 74LS08	U48
330-00703	2	IC, DIGITAL, 74LS74	U32,51
330-00708	1	IC, DIGITAL, 74LS107	U49
330-00711	2	IC, DIGITAL, 74LS157	U37,43
330-00716	2	IC, DIGITAL, 74LS283	U36,42
330-00718	4	IC, DIGITAL, 74LS367	U34,35,40,41
330-01293	3	IC, DIGITAL, 74LS374	U33,39,46
330-01295	2	IC, DIGITAL, 74LS393	U38,44
330-01282	2	IC, DIGITAL, 74LS138	U55,56
330-01577	1	IC, DIGITAL, 74LS191	U54
330-02085	1	IC, DIGITAL, 25L04	U45

6.3.2 MOTHERBOARD (CONT.)

PART NO.	QTY.	DESCRIPTION	REF.
INTEGRATED CIRCUITS CONT.			
340-00740	6	IC, LINEAR, RC4558	U5-8,60,61
340-01183	6	IC, LINEAR, LF356	U1,14,15,21,22,62
340-01566	6	IC, LINEAR, LF353	U4,9,10,11,12,16
340-01363	2	IC, LINEAR, LF339	U2,58
340-00728	1	IC, LINEAR, NE566	U59
340-00744	1	IC, LINEAR, 78L05C	U57
340-00733	1	IC, LINEAR, CA3039	U18
340-00725	2	IC, LINEAR, LM311	U3,20
340-00742	1	IC, LINEAR, 7805/340-T5	U64
340-00745	1	IC, LINEAR, 7815/340-T15	U13
340-00747	1	IC, LINEAR, 7915/320-T15	U24
340-02086	1	IC, LINEAR, LM317LH (OR MP)	U63
346-01366	2	IC, SWITCH, CD4016	U17,23
350-01299	6	IC, MEMORY, MCM4116	U25-30
350-02089	1	IC, MEMORY, 82S123 (CUST. MASK)	U47
355-02087	1	IC, CONVERTER, AM6012DC	U19
SWITCHES			
451-02230	1	SWITCH,SLIDE,2P2T,PC,VOLT CHANGEOVER	SW5
453-02226	1	SWITCH,PB,PP,2P2T,LINE RATED	SW6
453-02111	2	SWITCH,PB,PP,2P2T,ALPS	SW2,4
453-02112	1	SWITCH,PB,PP,10P2T,ALPS	SW1
453-02246	1	SWITCH,PB,PP,3GANG,2P2T,ALPS	SW3
MISC.			
430-02286	2	LAMP,LED, GREEN	CR38,39
440-00860	1	FUSE, 1/4A,3AG,SLO-BLO	F1
470-02110	1	XFORMER, POWER, 115/230	T1
490-00831	3	SOCKET, XSISTOR, 3 PIN,MOLEX	U13,24,64
510-00941	21	SOCKET, IC, 8 PIN	U1,3-12,14-16, 20-22,59-62
510-00942	13	SOCKET, IC, 14 PIN	U2,17,23,31,32, U38,44,48,49,51-53, U58
510-00943	18	SOCKET, IC, 16 PIN	U25-30,34-37,40-43, 47,54-56
510-01361	4	SOCKET, IC, 20 PIN	U19,33,39,46
510-00945	1	SOCKET, IC, 24 PIN	U45
510-02106	6	JACK,PHONE, PC,RT.ANGLE,3 COND	J1-3,6-8
510-01066	1	CONN.,WAFER, 10 PIN,MOLEX	J5
520-00798	1	CONN.,RECEPT.,EAC301	J9
600-00871	2	HDWR, FUSE CLIP, PC MTG.,3AG	F1
630-01894	1	SPACER, NYLON, TO-5	USED WITH U63

6.3.2 MOTHERBOARD (CONT.)

PART NO.	QTY.	DESCRIPTION	REF.
MISC. CONT.			
670-01684	1	WIRE, 18AWG, UL1015,16/30,BLK,6 1/2",STRIP 3/16"	
670-01683	1	WIRE, 18AWG, UL1015,16/30,WHT, 9", STRIP 3/16"	
670-01685	1	WIRE, 16AWG, UL1015,26/30,GRN, 3", STRIP 3/16"	
710-02186	1	BOARD, PC, MOTHER, PCM-41	
EUROPEAN AND RFI OPTION			
OMIT:			
440-00860	1	FUSE, 1/4A, 3AG, SLO-BLO	F1
520-00798	1	CONN.,RECEPT., EAC301	J9
600-00871	2	HDWR. FUSE CLIP, PC MTG., 3AG	
SUBSTITUTE:			
440-02347	1	FUSE, 1/8A, 20MM, SLO-BLO, LF213.125	F1
440-02349	2	FUSE, 1/2A, 20MM, SLO-BLO, LF213.125	F4,5
440-02350	2	FUSE, 2A, 20MM, SLO-BLO, LF213002	F2,3
520-00396	1	CONN., AC,CORCOM 1EF1 (IN PLACE OF EAC301)	J9
600-02227	10	HDWR. FUSE CLIP, PC MTG., 20MM	
JAPAN OPTION			
OMIT:			
440-00860	1	FUSE, 1/4A, 3AG, SLO-BLO	F1
520-00798	1	CONN.,RECEPT., EAC301	J9
470-02110	1	XFORMER, POWER, 115/230	T1
600-00871	2	HDWR. FUSE CLIP, PC MTG., 3AG	
SUBSTITUTE:			
440-02348	1	FUSE, 1/4A, 20MM, SLO-BLO, LF213.125	F1
440-02349	2	FUSE, 1/2A, 20MM, SLO-BLO, LF213.500	F4,5
440-02350	2	FUSE, 2A, 20MM, SLO-BLO, LF213002	F2.3
520-00396	1	CONN.,AC, CORCOM 1EF1 (IN PLACE OF EAC301	J9
470-02119	1	XFORMER, POWER, 100/200	T1
600-02227	10	HDWR. FUSE CLIP, PC MTG., 20MM	

6.3.3 H.R.I. BOARD

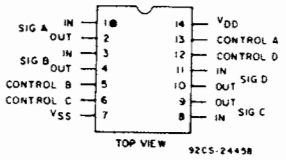
PART NO.	QTY.	DESCRIPTION	REF.
430-02285	1	LAMP,LED, RED	CR52
430-02286	3	LAMP,LED, GREEN	CR54-56
430-02287	1	LAMP,LED, YELLOW	CR53
510-01070	1/3	CONN.,WAFER,18 PIN,MOLEX 22-05-2181	P1
710-02200	1	PC BOARD, HRI, PCM-41	

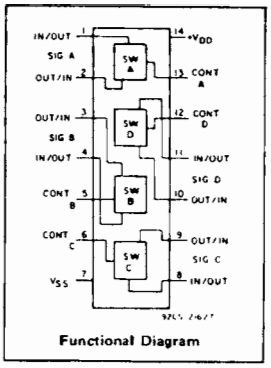
6.3.4 DISPLAY BOARD

PART NO.	QTY.	DESCRIPTION	REF.
202-00515	3	RES.,CF, 5%,1/4W, 150 OHM	R158-160
430-02285	11	LAMP, LED, RED	CR57-67
430-02287	2	LAMP, LED, YELLOW	CR68,69
453-02113	2	SWITCH,PBM,SPST,PETRICK " "	SW7,8
510-01070	1	CONN.,WAFER,18 PIN,MOLEX 22-05-2181	P2,3
710-02193	1	PC BOARD, DISPLAY, PCM-41	

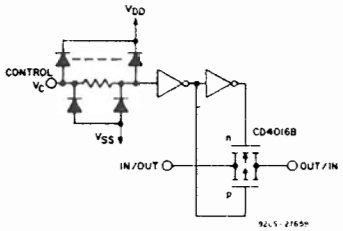
SECTION 6.4 I.C. LAYOUTS

Terminal Assignment





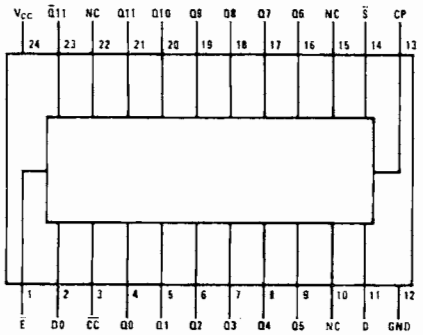
Functional Diagram



Schematic diagram - 1 of 4 identical sections.

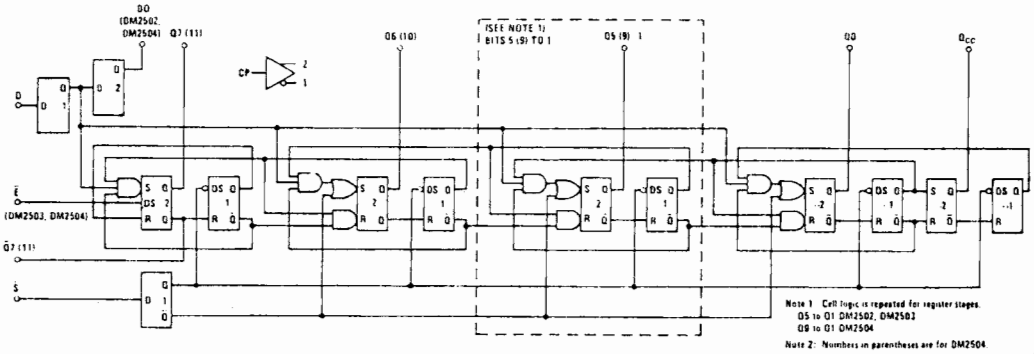
Connection Diagram

Dual-In-Line Package



25L04

Logic Diagram

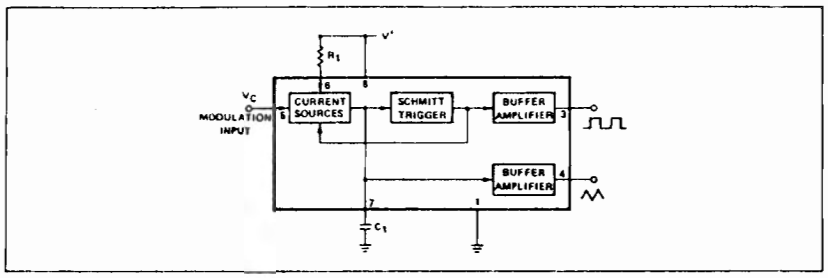


Truth Table

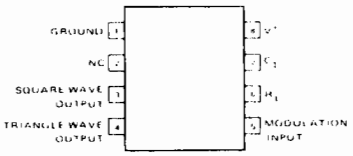
TIME	INPUTS			OUTPUTS													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

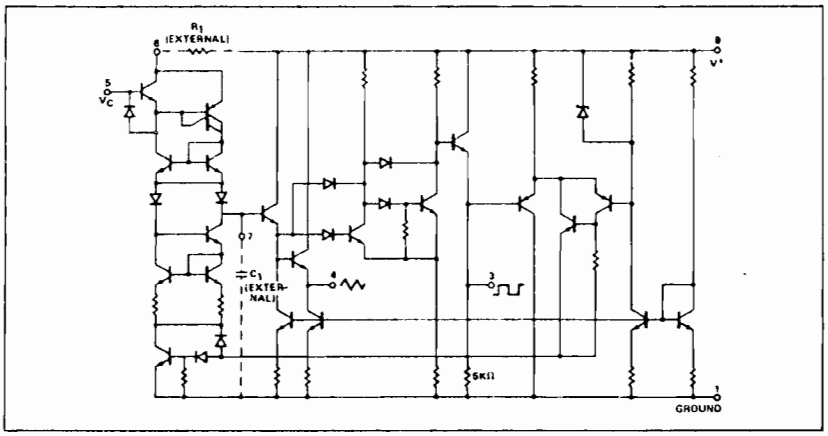
BLOCK DIAGRAM



N PACKAGE

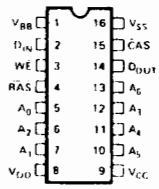


EQUIVALENT SCHEMATIC

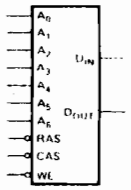


NE566

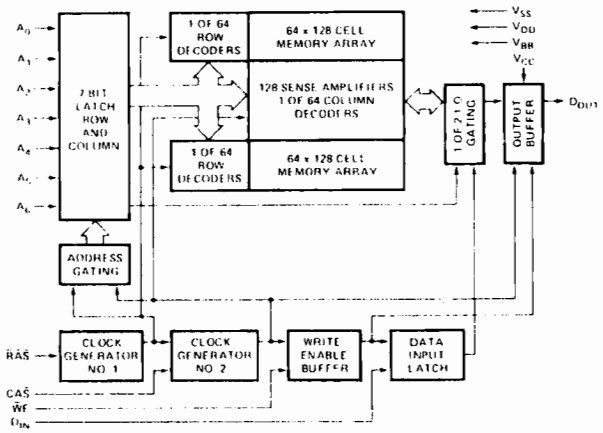
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM

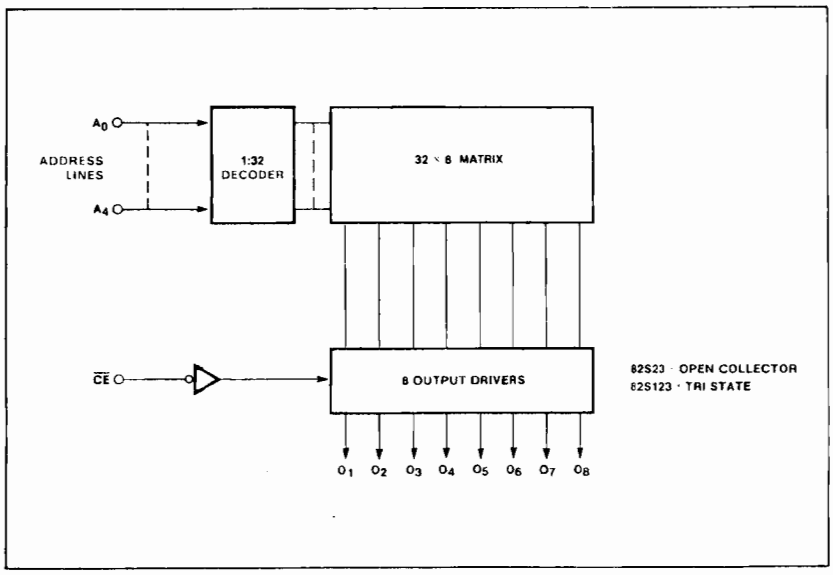


PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

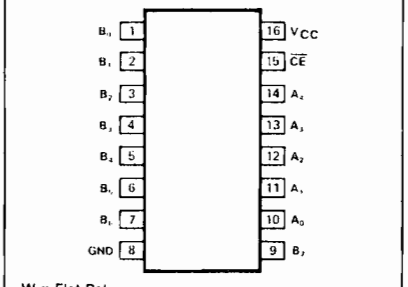
16K RAM

LOGIC DIAGRAM



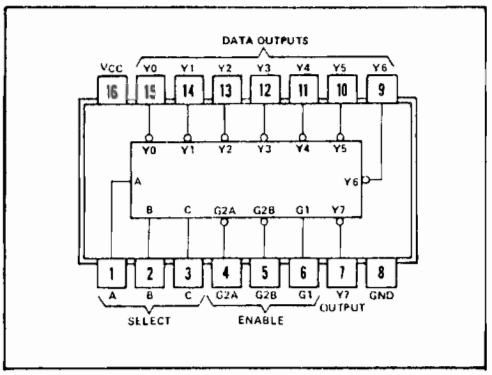
PIN CONFIGURATION

F,N,W, PACKAGE



W = Flat Pak
F = Cerdip
N = Plastic

82S123

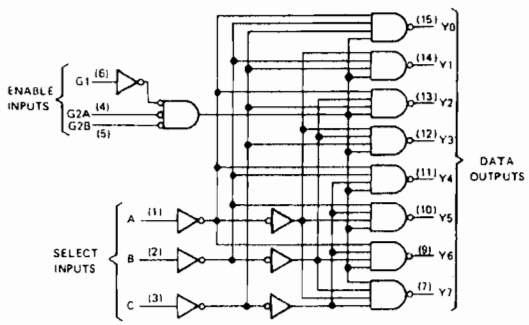


'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

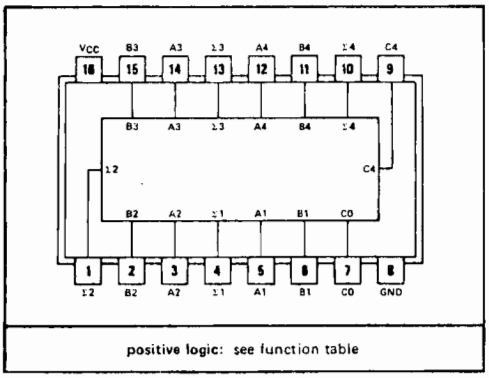
*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

'LS138, 'S138



74LS138

SN54283, SN54LS283 . . . J OR W PACKAGE
SN54S283 . . . J PACKAGE
SN74283, SN74LS283, SN74S283 . . . J OR N PACKAGE
(TOP VIEW)



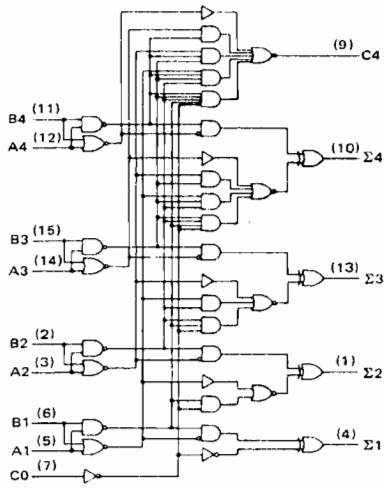
positive logic: see function table

FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

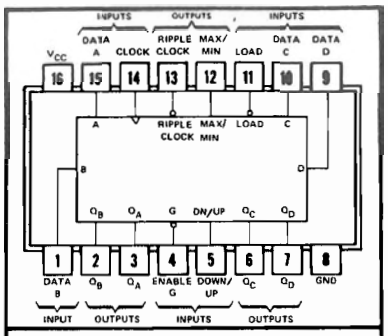
H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.



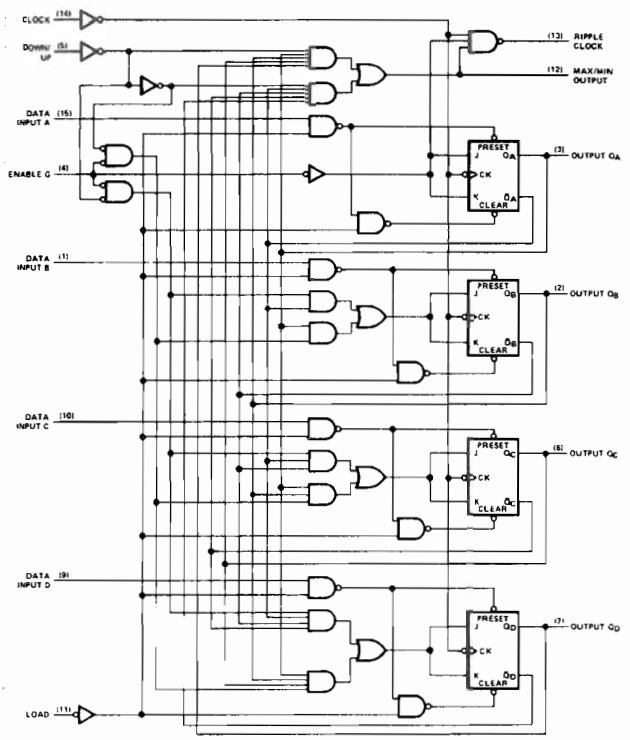
74LS283

SN54', SN54LS' . . . J OR W PACKAGE
SN74', SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



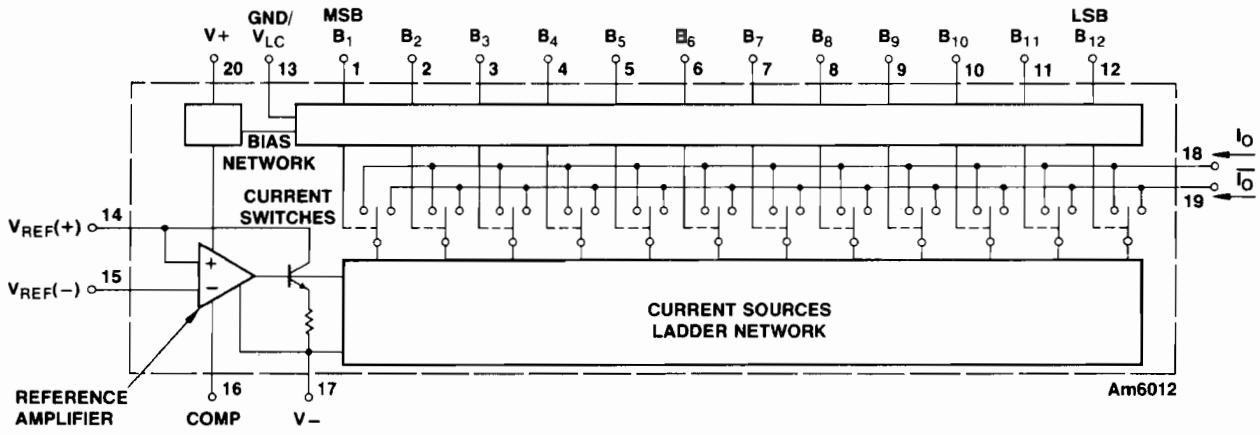
asynchronous inputs: Low input to load sets Q_A=A, Q_B = B, Q_C = C, and Q_D = D

'191, 'LS191 BINARY COUNTERS



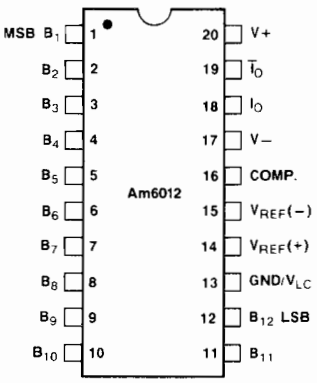
74LS191

FUNCTIONAL DIAGRAM



LIC-846

CONNECTION DIAGRAM — Top View



Note:
Pin 1 is marked for orientation.

LIC-847

AM6012DC

6.5 SIGNATURE ANALYSIS TABLES

NOTES:

$ Probe Tip Flashing

IC/PIN		SIGNAL NAME	SIGNATURE
U49	12	MC0	0000 $
	9	MC1	0003 $
	5	WC0	0001
U44	3	WC1	UUUU
	4	WC2	FFFF
	5	WC3	8484
	6	MA1	P763
	11	MA2	1U5P
	10	MA3	0356
	9	MA4	U759
	8	MA5	6F9A
U38	11	MA6	7791
	10	MA7	6321
	9	MA8	37C5
	8	MA9	6U28
	3	MA10	45CA
	4	MA11	4868
	5	MA12	9UP1
	6	MA13	0002
U47	1		22CC
	2		C8UA
	3		8U98
	4		4853
	5		8534
	6		534C
	7		71U0
	9		C8UA

NOTES:

* Signature obtained only when the particular line is selected by front panel
** Signature obtained if RPT/HOLD activated
*** Signature obtained on 0 delay setting

IC/PIN		SIGNAL NAME	SIGNATURE	
U46	2	RQCC1	915H	
	5	SEL LO/	HF7U	
	19	SEL HI/	F7FP	
	16	RDLO	A429	
	6	RDHI	429A	
	9	SC/	29A7	
	15	ISAM/	C8UA	
	12	OSAM/	HF7U	
U53	3		8484 (0-100)	0003 (200 ms)
U55	15	01	0003	8484*
	14	MIN/	0003	8484*
U36	6	OFS0	0003	8484*
	2	OFS1	0003	8484*
	15	OFS2	0003	8484*
	11	OFS3	0003	8484*
U42	6	OFS4	0003	8484*
	2	OFS5	0003	8484*
	15	OFS6	0003	8484*
	11	OFS7	0003	8484*
U56	13	MAX/	0003	8484*
U31	3	WR/	8487	0003**
	6	CAS/	5556	
	8	RAS/	UUUF	
	11		UUUF	
U48	6	LDLO	A429	
	8	LDHI	429A	
U52	3	MDE/	915P	0000***
	6	SARE/	915H	0003***

MEMORY TEST NO.1

NOTES:
~Signatures from this point taken with the comparator (U20) removed and SAR data jumpered to WC1

IC/PIN		SIGNAL NAME	SIG @ 1.6 ms DLY SETTING	SIG @ 13 ms DLY SETTING	SIG @ 200 ms DLY SETTING
U36	4	OMA6	7791	U316	7791
	1	OMA7	P7A6	5585	6321
	13	OMA8	2282	A2C3	37C5
	10	OMA9	H70H	37C9	6U28
U42	4	OMA10	U93C	2H87	4FCA
	1	OMA11	AF99	F6P7	4868
	13	OMA12	HF6U	AC2P	9UP1
	10	OMA13	CAP9	PFHP	0002
U37	4	A0	F42P		
	7	A1	2656		
	9	A2	774P		
	12	A3	641U		
U43	4	A4	C066		
	7	A5	1FAC		
	9	A6	4CHF		
U45	4	Q0	9A41~		
	5	Q1	3486~		
	6	Q2	5693~		
	7	Q3	8487~		
	8	Q4	A42A~		
	9	Q5	4850~		
	16	Q6	U85C~		
	17	Q7	H916~		
	18	Q8	4299~		
	19	Q9	8537~		
	20	Q10	14H0~		
	21	Q11	0000~		
DATA @ DAC			(0 ms)		
U19	1	DAC0	9A41		
	2	DAC1	3486		
	3	DAC2	5693		
	4	DAC3	8487		
	5	DAC4	A42A		
	6	DAC5	4850		
	7	DAC6	U85C		
	8	DAC7	H916		
	9	DAC8	4299		
	10	DAC9	8537		
	11	DAC10	14H0		
	12	DAC11	0000		

NOTES:

~ Signatures from this point taken with the comparator (U20) removed and SAR data jumpered to WC1
^ These signatures are for U25-U30
^^ Delay set @1.6ms

IC/PIN		SIGNAL NAME	SIGNATURE
U25	2	D0	31FH~
U26	2	D1	31FH~
U27	2	D2	31FP~
U28	2	D3	31FP~
U29	2	D4	31FH~
U30	2	D5	31FH~
^	3	WR/	8487~
^	4	RAS/	UUUF~
^	15	CAS/	5556~
^	5	A0^^	542P~
^	6	A1^^	2656~
^	7	A2^^	774P~
^	12	A3^^	641U~
^	11	A4^^	C066~
^	10	A5^^	1FAC~
^	13	A6^^	4CHF~
U39	9	DAC0	9A41~
	7	DAC1	3486~
	11	DAC2	5693~
	5	DAC3	8487~
	13	DAC4	A42A~
	3	DAC5	4850~
U40	9	DAC6	U85C~
	7	DAC7	H916~
	11	DAC8	4299~
	5	DAC9	8537~
	13	DAC10	14H0~
	3	DAC11	0000~

MEMORY TEST NO.2

NOTES:
These signatures taken with the comparator (U20) removed and SAR data jumpered to A6 (U43, pin 9).

IC/PIN		SIGNAL NAME	0 ms	13 ms	200 ms
U45	4	Q0	1575		
	5	Q1	FH8F		
	6	Q2	4529		
	7	Q3	253A		
	8	Q4	2138		
	9	Q5	73FA		
	16	Q6	0H35		
	17	Q7	9FA7		
	18	Q8	0A73		
	19	Q9	255H		
	20	Q10	7559		
	21	Q11	6F7U		
U25	2	D0	18H4	25AH	21P0
U26	2	D1	18H4	25AH	21P0
U27	2	D2	4504	982P	4U11
U28	2	D3	4504	982P	4U11
U29	2	D4	F07C	2521	21P0
U30	2	D5	F07C	2521	21P0
U34	9	DAC0	1575	8P1H	1575
	7	DAC1	FH8F	56P4	FH8F
	11	DAC2	4529	H474	4529
	5	DAC3	253A	C467	253A
	13	DAC4	2138	H9PU	H856
	3	DAC5	73FA	5H4F	57FC
U40	9	DAC6	0H35	9F68	65FC
	7	DAC7	9FA7	0HUA	64UU
	11	DAC8	0A73	639A	0A6A
	5	DAC9	255H	29A7	U3C2
	13	DAC10	7559	P404	6CP2
	3	DAC11	6F7U	UH22	78AF

DATA @ DAC			0 ms
U19	1	DAC0	1575
	2	DAC1	FH8F
	3	DAC2	4529
	4	DAC3	253A
	5	DAC4	2138
	6	DAC5	73FA
	7	DAC6	0H35
	8	DAC7	9FA7
	9	DAC8	0A73
	10	DAC9	255H
	11	DAC10	7559
	12	DAC11	6F7U

DELAY SELECT LOGIC TEST PROCEDURE

NOTES:
* Point being probed is not the selected delay
** Point being probed corresponds to the selected delay

IC/PIN		SIGNAL NAME	SIGNATURE	NOTES
U51	3	MA9	6U28	
	11	MA9	6U28	
	2		0003	Probe lamp goes out when [<-] is pushed.
	12		0003	Probe lamp goes out when [->] is pushed.
	9		0003	Probe lamp goes out when [->] is pushed.
	5		0003	Probe lamp goes out when [<-] is pushed.
U52	8		0003	Probe blinks off when [<-] is pushed.
	8		0003	Probe blinks off when [->] is pushed, except in 200/400 ms position.
	9			Probe blinks on when [<-] is pushed.
	9			Probe blinks on when [->] is pushed, except at 200 ms.

NOTE: For the probe tests that follow for U54 QA, QB, QC, and QD outputs, the delay display cannot be assumed to be working. For that reason, a truth table is given.

U54	4	ZERO		Probe lamp on only in 0 delay position.
	3			Probe lamp on for .8, 2.4, 7.0, 26, 100
	2			Probe lamp on for 1.6, 2.4, 13, 26, 200
	6			Probe lamp on for 4, 7, 13, 26
	7			Probe lamp on for 50, 100, 200

		FUNCTION	DELAY SETTING	TRUTH TABLE QD	QC	QB	QA	SIGNATURE	
U55	15	0	0 ms	0	0	0	0	0003*	8484**
	14	MIN/	.8	0	0	0	1	0003*	8484**
	13	OFS0	1.6	0	0	1	0	0003*	8484**
	12	OFS1	2.4	0	0	1	1	0003*	8484**
	11	OFS2	4.0	0	1	0	0	0003*	8484**
	10	OFS3	7.0	0	1	0	1	0003*	8484**
	9	OFS4	13.0	0	1	1	0	0003*	8484**
	7	OFS5	26.0	0	1	1	1	0003*	8484**
U56	15	OFS6	50.0	1	0	0	0	0003*	8484**
	14	OFS7	100.0	1	0	0	1	0003*	8484**
	13	MAX	200.0	1	0	1	0	0003*	8484**

U48	12		0003	Probe lit.
	13		0003	Probe lit.
	11		0003	Probe lit.
U53	1	MAX/	0003 (0-100 ms)	8484 (200 ms)
	2		8487	
	3		8484 (0-100 ms)	0003 (200ms)
	4	WC3	8484	
	5	WC3	8484	
	6		8487	

7.0 RETURNING UNITS FOR REPAIR

If it becomes necessary to return a PCM-41 for service, bear in mind that Lexicon assumes no responsibility for units in shipment from customer to factory, whether in or out of warranty. It is important, therefore, that shipments be well packed, properly insured, and consigned to a reliable agent, such as UPS or Federal Air Express. Be sure to include (in the carton) a note explaining the nature of the problem, referencing any conversation with Lexicon personnel, detailing the preferred shipping method, and indicating a date when the unit is needed again. Do not include accessories such as power cords, manuals, and remote switches. It is also important to provide Lexicon with the name and telephone number of a person we may contact should any questions arise.

7.1 REPLACEMENT PARTS

Replacement parts may be ordered from:

Lexicon, Inc.
60 Turner Street
Waltham, MA 02154
U.S.A.
Attn: Customer Service Dept.

Parts will be shipped FOB Waltham.

Charges will be that price in effect at the time the order is received. Lexicon may be consulted at any time, during business hours, for a parts quotation.

When ordering parts, refer to the appropriate parts list in the PCM-41 Service Manual or order by complete description and give the following information:

A. Assembly - Motherboard, Chassis, HRI, Display

B. Part No. and I.D. if available.

C. Item Description

D. Quantity Desired

E. PCM-41 Serial No., if available

7.2 LIMITED WARRANTY

Lexicon warrants each PCM-41 to be free from defects in material and workmanship under normal use and service for one year. This warranty begins on the date of delivery to the purchaser or his authorized agent or carrier. During the warranty period, Lexicon will repair, or at its option, replace at no charge, components that prove to be defective provided the equipment is returned, shipping prepaid, to Lexicon's factory or designated service facility.

This warranty is null or void under any of the following conditions:

a. Abuse, neglect, alteration, or repair by unauthorized personnel.
b. Damage caused by improper use, or operation from an incorrect power source.
c. Damage caused by accident, act of God, war, or civil insurrection.

Lexicon shall not be responsible for any loss or damage, direct or consequential, resulting from machine failure or the inability of the product to perform. Lexicon shall not be responsible for any damage or loss during shipment to or from the factory or its designated service facility.

This warranty is in lieu of all other warranties, expressed or implied, and of any other liabilities on Lexicon's part, and Lexicon does not assume or authorize anyone to make any warranty or assume any liability not strictly in accordance with the above.

Lexicon reserves the right to make changes or improvements in the design and constructon of the machine without obligation to make such changes or improvements in the purchaser's machine.

No equipment may be returned under this warranty without prior authorization from Lexicon. Authorized return shipments must be prepaid and should be insured. Systems modules being returned for repair/exchange should be wrapped or packed in soft packing material and shipped in an appropriate small protective box. In the case of returning the entire machine, it should be carefully packed in the original carton and packing material. If this is not available, new ones may be procured from Lexicon.

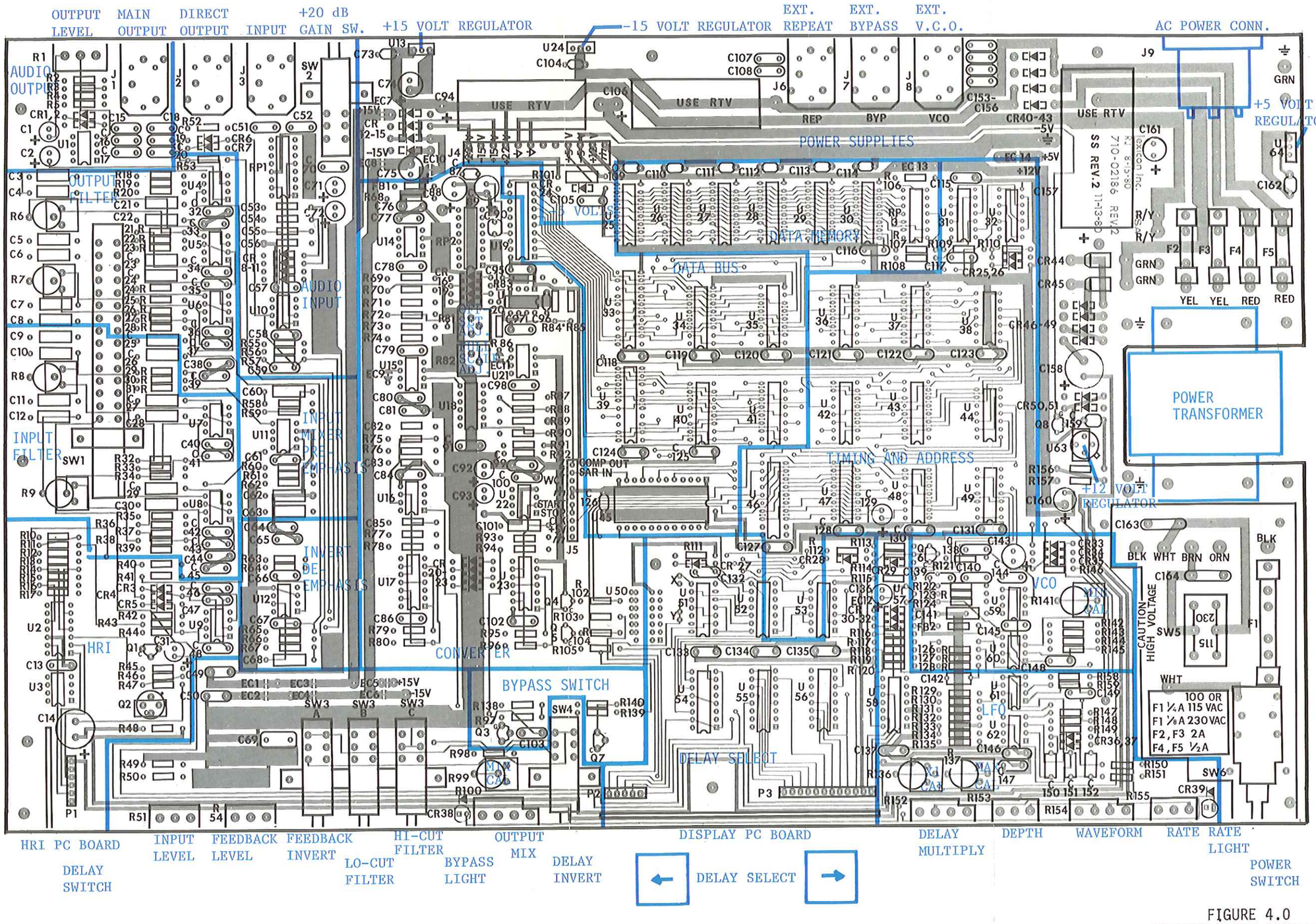


FIGURE 4.0
CIRCUIT BLOCK LOCATIONS

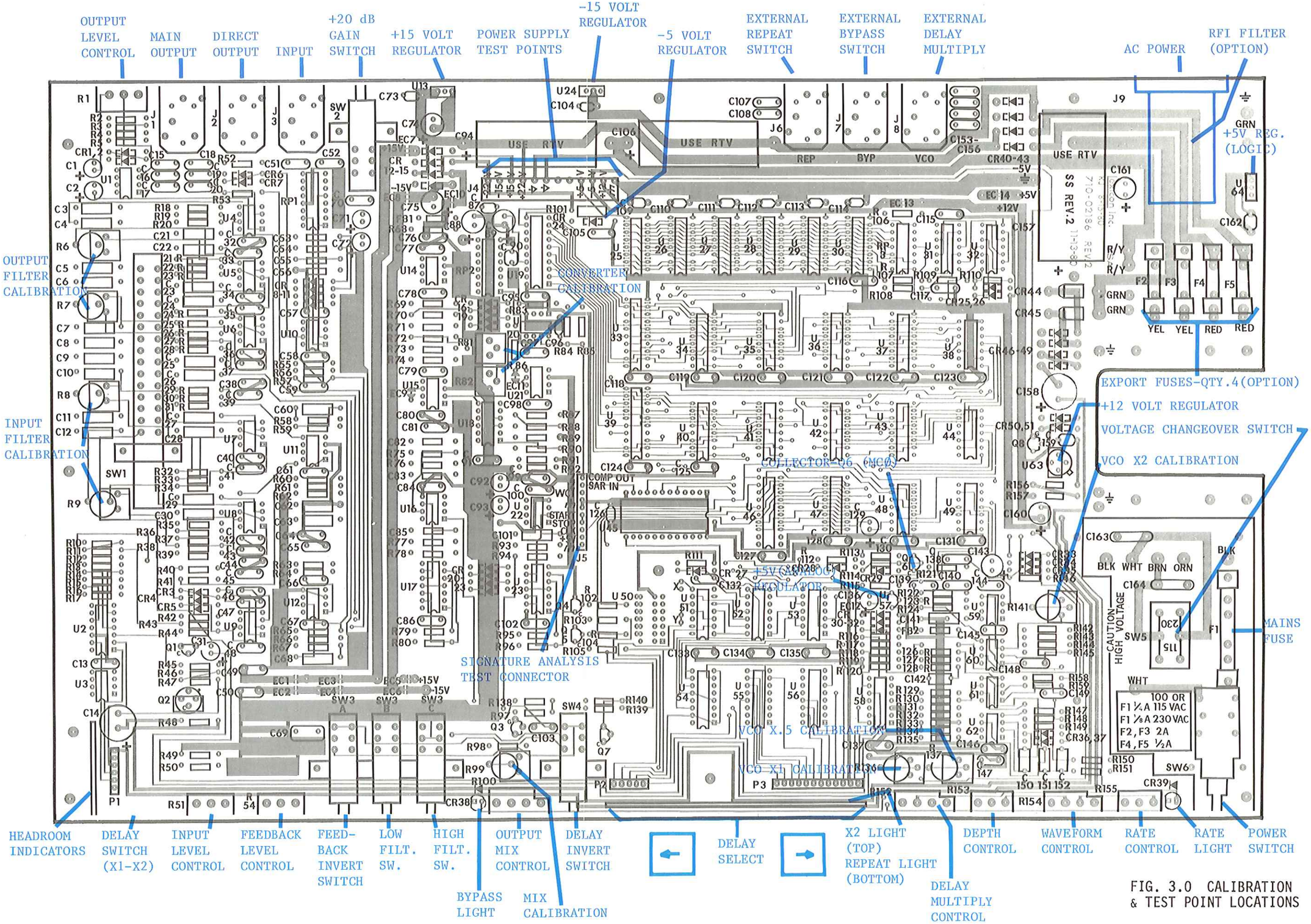


FIG. 3.0 CALIBRATION & TEST POINT LOCATIONS

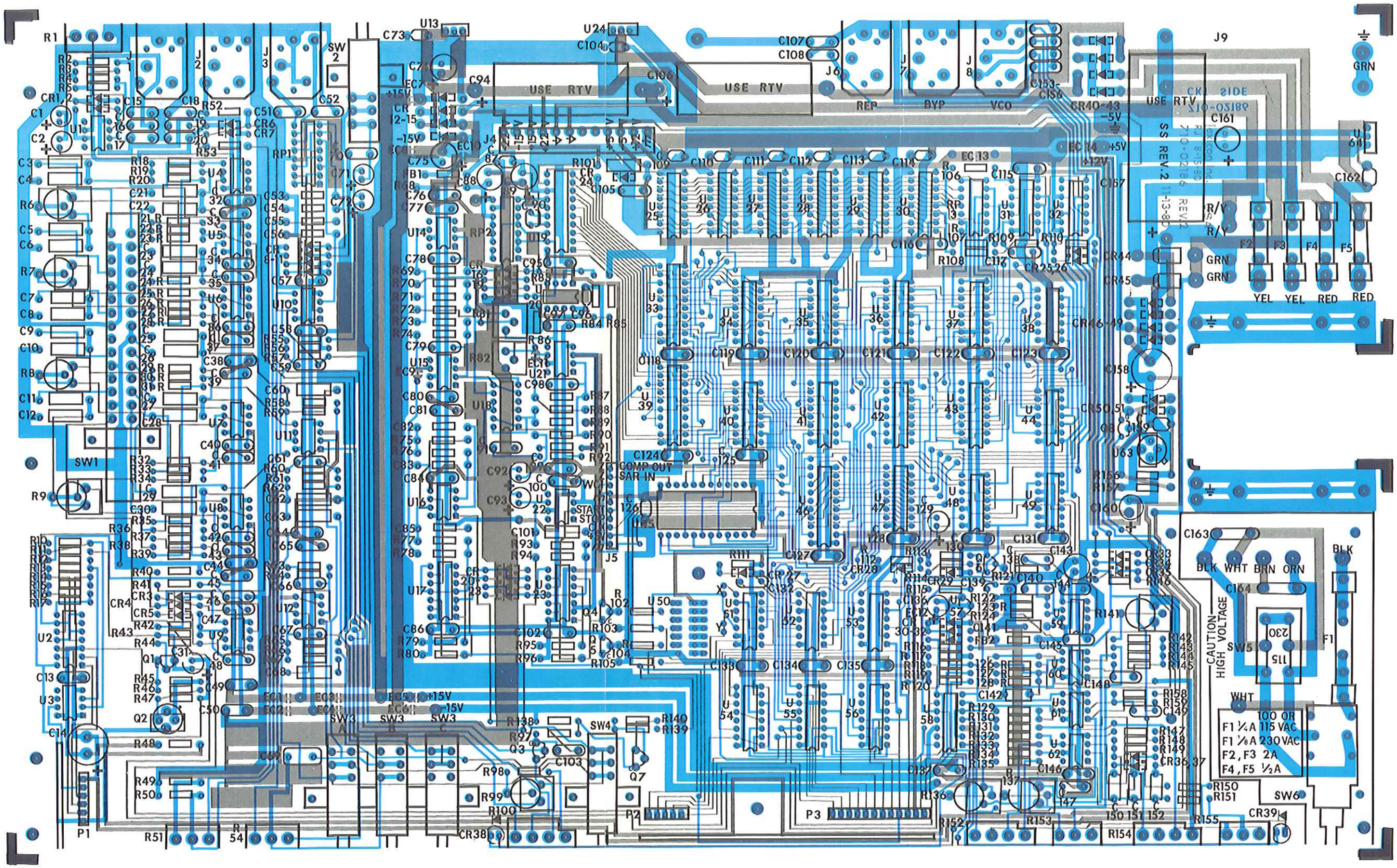


FIGURE 6.1 INTERIOR LAYOUT

REVISIONS					
REV.	DESCRIPTION			DATE	APPROVED
	PART	WAS	NOW		
1	R4	3.3K	6.2K	1/20/81	R.J.
	R10	1 MEG	2MEG		
	R55	750Ω	620Ω		
	R56	10K	7.5K		
	R61	9.53K	9.31K		
	Q3	E113	J113-10		
2	ADD NOTES 4 & 5			4/23/81	JMG
	U2 WAS LF339, NOW LM 339. REVERSE POT ORIENTATION, R6 - R9				

NOTES

1. DIGITAL GND ⏚ ANALOG GND ⏚
2. CAPACITORS IN µF/VOLTS UNLESS OTHERWISE INDICATED
3. ALL DIODES ARE IN4148
4. XY/AB DENOTES PRINT NO. AND INTERSECT COORDINATE (PRINT NO. IS 060-0217XY)
5. ON BOARD CONNECTION TO → FROM ←

QTY REQ'D	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
			PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX NA .XXX NA	CONTRACT NO.		lexicon
	APPROVALS	DATE	SCHEMATIC, ANALOG SECTION, 41
MATERIAL NA	DRAWN EXSMITH	11/17/80	
FINISH NA	CHECKED R.J.	1/20/81	SIZE D | FSCM NO. | DWG. NO. 060-02178-D | REV. 2
NEXT ASSY | USED ON	ISSUED		SCALE NA | SHEET 1 OF 1
APPLICATION	DO NOT SCALE DRAWING		

41

FIG. 6.2.1

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1.	CR20 WAS 4148, NOW SCHOTTKY DIODE	1/20/81	JM/RJ.

NOTES

1. RESISTORS ARE 5%, 1/4W UNLESS OTHERWISE INDICATED.
2. CAPACITOR VALUES IN μF/V UNLESS OTHERWISE INDICATED.
3. CR20 IS DIODE, SCHOTTKY, BAR35; ALL OTHER DIODES ARE IN4148.
4. DIGITAL GND. ANALOG GND.
5. XY/AB DENOTES PRINT NO. AND INTERSECT COORDINATE. (PRINT NO. IS 060-021XY".)
6. ON BOARD CONNECTION: TO / FROM

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX NA	CONTRACT NO.		lexicon
MATERIAL NA	APPROVALS	DATE	SCHEMATIC, CONVERTER, 41
FINISH NA	DRAWN Ellen G.	12/23/80	
DO NOT SCALE DRAWING	CHECKED R.T.	1/20/81	SIZE C · FSCM NO. · DWG. NO. 060-02184-C · REV. 1
	ISSUED		SCALE NA · SHEET 1 OF 1

NEXT ASSY	USED ON
	41
APPLICATION	

FIG. 6.2.2

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1.	ADD +5V TO TEST CONN.	3/6/81	SG/R.J.
2.	DELETE C108 ADD CHIP DATA U32, 34, 36, 40, 46	4/24/81	SG/

NOTES

1. RESISTORS ARE 5%, ¼W
   CAPACITORS VALUES ARE IN μF UNLESS OTHERWISE INDICATED.
   DIODES CR57-69 ARE LAMP, LED
   ALL OTHER DIODES ARE 4148.
2. ⏚ DIGITAL GND ▽ ANALOG GND A7Ø8 SIGNATURE NAME
3. XY/AB DENOTES PRINT NO. AND INTERSECT COORDINATE (PRINT NO. IS 060-021'XY')
4. ON BOARD CONNECTION TO → FROM →
5. ALL SIGNATURES GIVEN FOR 1.6MS DELAY NOT REPEAT MODE (U20 REMOVED & WC1 CONNECTED TO PIN 11 OF U45), REFER TO SIGNATURE TABLE FOR ADDITIONAL INFORMATION.
6. ALL SIGNATURES TAKEN USING HP5004A OR EQUIVALENT.

QTY REQ	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
XX NA
XXX

MATERIAL NA
FINISH NA
DO NOT SCALE DRAWING

CONTRACT NO.

Lexicon

APPROVALS	DATE
DRAWN GUROSHIM	10/3/80
CHECKED CB	11/19/80
ISSUED CB	11/19/80

SCHEMATIC, DIGITAL SECTION, 41

SIZE D | FSCM NO. | DWG. NO. 060-02180-D | REV. 1

SCALE NA | SHEET 1 OF 1

41 | NEXT ASSY | USED ON | APPLICATION

FIG. 6.2.3

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1.	CHANGE BYPASS & EXTERNAL VCO TO BE COMPATABLE WITH MODEL 93 : CIRCUITS ASSOCIATED WITH USB, PIN 8,9&14; U61 PIN 1,2&3; ALSO C162 WAS .1/50, NOW 4.7/25	1/20/81	/RK
2.	PART: CR24 R146 R157 — WAS: IN750 5.1K — NOW: IN751 10K 499Ω	3/6/81	SG/R.J.
3.	R154 WAS "SHAPE", NOW WAVEFORM"; ADD RF. FILTER DETAIL	4/23/81	SG/

NOTES

1. RESISTORS ARE 5%, ¼W UNLESS OTHERWISE INDICATED.
2. CAPACITOR VALUES IN UF/V UNLESS OTHERWISE INDICATED.
3. POWER SUPPLY DIODES IN4004 UNLESS OTHERWISE INDICATED. CONVERTER DIODES 4148 UNLESS OTHERWISE INDICATED.
4. ⏚ DIGITAL GND ⏚ ANALOG GND
5. XY/AB DENOTES PRINT NO. AND INTERSECT COORDINATE. (PRINT NO. IS 060-021XY.)
6. ON BOARD CONNECTION: TO / FROM

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX NA XXX	CONTRACT NO.		lexicon
MATERIAL NA	APPROVALS	DATE	SCHEMATIC, VCO & POWER SUPPLY, 41
FINISH NA	DRAWN GOLDSMITH	10/28/80	
DO NOT SCALE DRAWING	CHECKED R.J.	1/29/81	SIZE D — FSCM NO. — DWG NO. 060-02182-D — REV. 3
	ISSUED		SCALE NA — SHEET 1 OF 1

	41
NEXT ASSY	USED ON
APPLICATION	

FIG. 6.2.4

lexicon

60 Turner Street, Waltham, Massachusetts 02154/Telephone:(617) 891-6790

 Price $40.00

Doc.#070-02662 SEP 81 RJ